

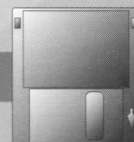


PEELTM
Products
Data Book



22 LV10
18 LV8

Includes PLACE
Software Manual



1995 / 1996

Data Book

General Information

PEEL Arrays

PEEL Devices

Special Products and Services

Development Tools

Application Notes and Reports

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PLACE Users Manual

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General Information

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General Information

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ICT Product Overview

ICT Inc. offers the most flexible PLD solutions for lower pin-count applications. ICT's Programmable Electrically Erasable Logic PEEL™ products include PEEL Devices, PEEL Arrays and PEEL Development Tools.

PEEL Product Features

- Most extensive PLD architecture offering in 20-44 pins
- CMOS EE technology for reprogrammability in cost effective plastic packaging
- Direct "JEDEC file-compatible" replacement and super-set replacement of popular PALs, GALs, and EPLDs
- Flexible architectures with more logic for new designs or design retrofits
- Speeds as fast as 5ns, low/zero-power and commercial/industrial versions
- DIP, PLCC, SOIC, TSSOP packaging
- Free PLACE™ Development Software
- Free Fitter Software for Synario, ABEL, CUPL, LOG/iC and OrCAD
- Free "PAL-GAL-EPLD-to-PEEL" Translation Software
- All devices supported by popular third-party programmers and ICT's PDS-3 programmer

PEEL Devices	PEEL Arrays	Development Tools
PEEL16V8	PA7024	PLACE Advanced Development Software
PEEL18CV8	PA7128	PEEL Array Fitters: ABEL-to-PEEL ABEL(WIN)-to-PEEL Synario-to-PEEL CUPL-to-PEEL OrCAD-to-PEEL LOG/iC-to-PEEL
PEEL20V8	PA7140	PEEL "Smart" Translator
PEEL22CV8		PDS-3 PEEL Development System
PEEL20CG10A		
PEEL22CV10A		
PEEL22CV10AZ		
PEEL22LV10AZ		

Figure 1. ICT Product Line

PEEL Devices

ICT's PEEL Devices can replace standard 20 and 24-pin PLDs like PALs, GALs and 22V10s. With additional architectural features (more inputs, product terms, macrocell functions) they allow more logic to be put into every part.

PEEL Device products include the PEEL 16V8, 18CV8, 20V8, 22CV8, 20CG10A and 22CV10A which are offered in speed ranges from 5 to 25ns tpd. They have lower power consumption than most standard PLDs (as low as 10mA typical I_{CC} at 25MHz), with zero-power versions to be introduced.

PEEL Arrays

PEEL Arrays are Complex PLDs (CPLDs) with advanced architectural features packed into 24, 28 and 44 pin packages. The PEEL Array CPLD architecture combines a large programmable logic array (PLA) with FPGA-like logic cells to offer a flexible alternative to simple PALs/GALs, and CPLDs with segmented PAL-like blocks. Key PEEL Array architectural features include:

- Complete input/feedback availability
- Real PLA product term sharing
- True I/O buried registers with FPGA-like logic cells
- Multiple functions per logic cell (equal to 2-3 PLD macrocells)
- Flexible registers with independent or global clocks
- Independent output enables with sum-of-products control

The PEEL Array family includes the PA7024, PA7128 and PA7140 in 24, 28 and 40/44 pin packages respectively. They offer 36-60 registers/latches and 36-72 sum-of-products output functions. Wide-gate symmetrical timing is as fast as 9ns/15ns (internal/external) for combinatorial logic and as fast as 80MHz for sequential functions. Rich in input latches, buried registers and sum-of-product functions, PEEL Arrays are ideal for counters, state machines, comparators, glue logic and PAL/GAL/EPLD integration and superset replacement.

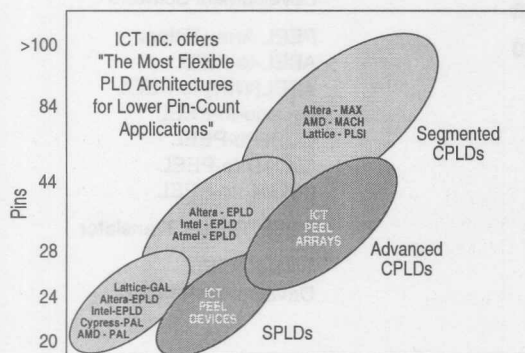


Figure 2. Architectural Flexibility/Density

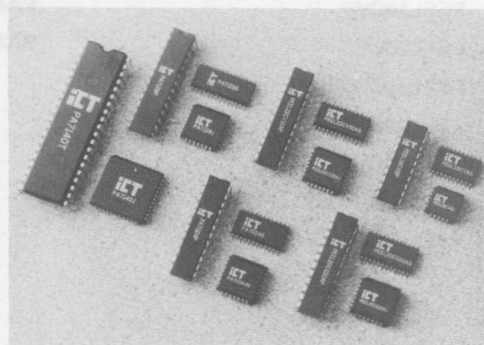


Figure 3. ICT PEEL Devices and Arrays

PEEL Products Selection Guide

	Architecture						Speed	Power		Key Features
	Pins	Inputs	I/Os	Registers	Macro Config	Product Terms	Tpd (ns) (min)	Icc(mA) (Typ)	Icc(mA) (Max)	
PEEL Device - Direct Replacement										
PEEL16V8	20	8	8	8	4	64	25, 15 10, 7, 5	45 - 75	55 - 115	Pin/JEDEC compatible with PAL/GAL 16V8/20V8, Q/L power versions
PEEL20V8	24	12								
PEEL22CV10A	24	12	10	10	4	132	25, 15 10, 7, 5	40 - 100	67 - 155	Pin/JEDEC file compatible with standard 22V10s, Low/Zero power
PEEL22CV10AZ								25µA (3.5@ 1MHz)	100µA (5.0@ 1MHz)	
PEEL Device - Superset Replacement										
PEEL18CV8	20	10	8	8	12	74	25, 15 10, 7, 5	18 - 75	37 - 110	Pin-comp. superset of 20/24-pin PAL/GAL/ EPLD, lower power
PEEL22CV8	24	14						10 - 75	15 - 90	
PEEL20CG10A	24	12	10	10	12	92	25, 15 10, 7, 5	40 - 100	67 - 155	Pin compatible superset of 24-pin PAL/GAL/EPLD
PEEL22CV10A+*	24	12	10	10	12	132	25, 15 10, 7, 5	40 - 100	67 - 155	Pin comp. superset of 22V10s, 12-config. macrocell
PEEL22CV10AZ+*							25, 15	25µA (3.5@ 1MHz)	100µA (5.0@ 1MHz)	Zero power version has P-term clock/ clock polarity
PEEL Arrays					Logic Functions					
PA7024	24	2	20	40 20 buriable	40	84 80 shared	15, 20, 25	85	120	Pin-comp. superset EP610, GAL6001
PA7128	28	14	12	36 24 buriable	36	67 64 shared	15, 20	75	105	Pin-compatible superset of 26V12, 24V10 & 26CV12
PA7140	40/44	14	24	60 48 buriable	72	125 60 shared	20, 25	80	100	Pin-comp. superset of EP910, more logic than EPM7032/ MACH 110.

* The "+" indicates the "plus" mode, a software/programming option allowing the 22CV10A and 22CV10AZ to use extra architecture features.

PEEL Development Tools

ICT's powerful PLACE Development Software (free to qualified PLD designers) provides everything a designer needs to develop custom logic designs for PEEL products. PLACE includes an architectural editor, logic compiler, waveform simulator, and a programmer interface. ICT also offers free PEEL Translation Software that automatically converts existing PAL, GAL and EPLD designs to PEEL Devices and PEEL Arrays.

Popular third-party PLD development software such as Synario, ABEL, CUPL, LOG/iC and OrCAD support ICT's standard PEEL Devices directly, and PEEL Arrays through ICT's free PEEL Array Fitters. All popular third-party programmers support PEEL products. For PLD users who need a programmer, ICT offers the PDS-3 PEEL Development System Programmer, a complete and cost-effective programming solution for all PEEL Devices and PEEL Arrays.

ICT Quality and Reliability

ICT, Inc. is dedicated to the design, manufacture, and marketing of user-programmable integrated circuits that exceed customer requirements through a continuous commitment to quality and customer service.

Customer Service

ICT is committed to providing quality products and service to our customer's expectations. At ICT, customer service plays an important role in quality assurance. All ICT employees are a part of the customer service team, whose goal is to provide complete customer satisfaction. ICT's commitment to this effort includes: expediting on-time deliveries, providing quick access to and action by our customer service department, keeping our sales, marketing and applications organizations well-trained for product support, publishing accurate and informative product documentation, addressing customer concerns and processing corrective actions, and ensuring that customer quality, reliability and service is kept in mind from design through production.

Quality and Reliability by Design

ICT's design philosophy emphasizes quality and reliability during every part of the design cycle. Conservative design rules and extensive logic and circuit simulation are performed over extreme operating conditions. During circuit and process design, special attention is paid to problems such as CMOS latch-up and electrostatic discharge (ESD). For example, ICT's I/O pins are prevented from CMOS latch-up by a double guard-ring designed into all products. Also ICT designers have developed and implemented techniques to protect all products from electrostatic discharge (ESD) up to 2000V on all I/O pins.

Initial Device Qualification

Tests have been developed to observe the life expectancy of each new product. In order to qualify a new product, packaged parts from a minimum of three different lots must be scrutinized for electrical functionality and reliability over extreme temperature and voltage conditions. Tests include operating life, data retention, endurance, temperature cycling, 85/85, ESD and latch-up. Pre-determined reliability goals must be met in order for a product to pass qualification. All procedures and results are carefully documented for future reference. This qualification validates the device, package and supplier. When design rules are adjusted, a new foundry or assembly facility is used, or a new package type is introduced, a re-qualification of the product is addressed. (For more information see Reliability Report RR-1 in Section 6 of the Data Book.)

Ongoing Monitor Qualification

Although initial device qualification is an essential step to a product release, all products are constantly monitored to ensure the reliability of the device. Production lots are sampled every quarter, and are subject to the same qualification tests. All results are again documented, and failures are carefully analyzed in order to find long term improvements to the product.

Quality and Reliability by Test

ICT has developed a test flow to ensure that all products shipped to customers are of the highest quality and reliability. Each device is erased, programmed and read at Wafer Sort, Post-Bake Final Test, Package Test and QA Test to guarantee electrical and functional characteristics of the part over the entire operating temperature range. Test programs are developed to screen out those devices which fail to meet data sheet specifications. Additionally, since all of ICT's products are programmable, every unit shipped is subjected to a data retention bake which verifies the ability to retain data for at least ten years over the entire temperature range. This is the equivalent of over forty years of data retention at 55°C.

Ongoing Monitor Qualification

Although initial device qualification is an essential step to a product release, all products are constantly monitored to ensure the reliability of the device. Production lots are sampled every quarter, and are subject to the same qualification tests. All results are again documented, and failures are carefully analyzed in order to find long term improvements to the product.

Quality and Reliability by Test

ICT has developed a test flow to ensure that all products shipped to customers are of the highest quality and reliability. Each device is assessed, programmed and tested at White Box, Post-Bake First Test, Package Test and QA Test to guarantee electrical and functional characteristics of the part over the entire operating temperature range. Test programs are developed to screen out those devices which fail to meet these exact specifications. Additionally, since all of ICT's products are programmable, every unit shipped is subjected to a data retention test which verifies the ability to retain data for at least ten years over the entire temperature range. This is the equivalent of over thirty years of data retention at 55°C.

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Introduction to PEELTM Arrays

2

Features

- **Programmable Electrically Erasable Logic Arrays**
 - Family of medium-density CPLDs
 - Reprogrammable CMOS EEPROM Technology
 - 24 to 44 pins in DIP, PLCC, and SOIC packages
- **Versatile Programmable Logic Array**
 - PLA structure with true product-term sharing
 - Logic, registers, latches can be I/O buried
 - 40 to 60 registers/latches
 - 40 to 72 logic cell output functions
- **Most Flexible Logic Cell of all CPLDs**
 - Multiple output functions per cell
 - D,T and JK registers with special features
 - Independent or global clocks, resets, presets, clock polarity, and output enables
 - All controls allow sum-of-products logic
- **High-Speed Wide-gate Performance**
 - tpd as fast as 9ns/15ns (internal/external)
 - fmax as fast as 76.9MHz
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
 - Integration of multiple PLDs and random logic
 - Buried counters, complex state-machines
 - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
 - Familiar PLD development methodology
 - ICT PLACE Development Software (free to qualified PLD designers)
 - Fitters for ABEL, CUPL, and other PLD Software
 - Programming support by ICT PDS-3 and other popular 3rd party programmers

Overview

Programmable Electrically Erasable Logic (PEEL) Arrays are a family of Complex Programmable Logic Devices (CPLDs) based on ICT's CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and the speed needed for today's programmable logic designs.

The PEEL Array family consists of three parts in packages ranging from 24 to 44 pins in plastic DIP, PLCC, and SOIC formats. ICT's CMOS EE technology allows reprogrammability and high-speed performance. Wide-gate delays as fast as 9ns for internal (buried) and 15ns external (pin to pin) are possible with PEEL Arrays. Clock frequencies can be as fast as 76.9MHz for sequential functions.

The PEEL Array architecture is based on a versatile multi-level programmable logic array (PLA) architecture rich in input latches, buried registers and sum-of-product logic functions. The PLA logic array structure provides (programmable AND, programmable OR) allowing true product term sharing.

PEEL Arrays offer the most flexible logic and I/O cells of any CPLD available today. The FPGA-style PEEL Array logic cell incorporates multiple outputs allowing registers and combinatorial logic

to be buried without limiting the use of I/O pins as with other CPLDs. Logic cell registers are user-configurable to be true D, T and JK registers with independent or global clocks, resets, presets, clock polarity and other special features. Additionally, all registers and output enables allow full sum-of-products control.

PEEL Arrays are ideal for implementing a wide variety of general purpose combinatorial, synchronous and asynchronous logic applications, including: buried counters, complex state-machines, comparitors, decoders, encoders, adders, address/data demux and other wide-gate logic. Because PEEL Arrays allow for multi-level buried logic, designs normally requiring multiple PLDs and/or random logic can be efficiently integrated.

Development support for PEEL Arrays is provided by ICT and popular third party development tool manufacturers. ICT offers the powerful PLACE Development Software (free to qualified PLD designers) complete with architectural editor, logic compiler, and waveform simulator. Development with ABEL, Synario, CUPL and OrCAD is accommodated by PEEL Array fitters from ICT. Programming for PEEL Arrays is supported by ICT's PDS-3 and other popular third party programmers.

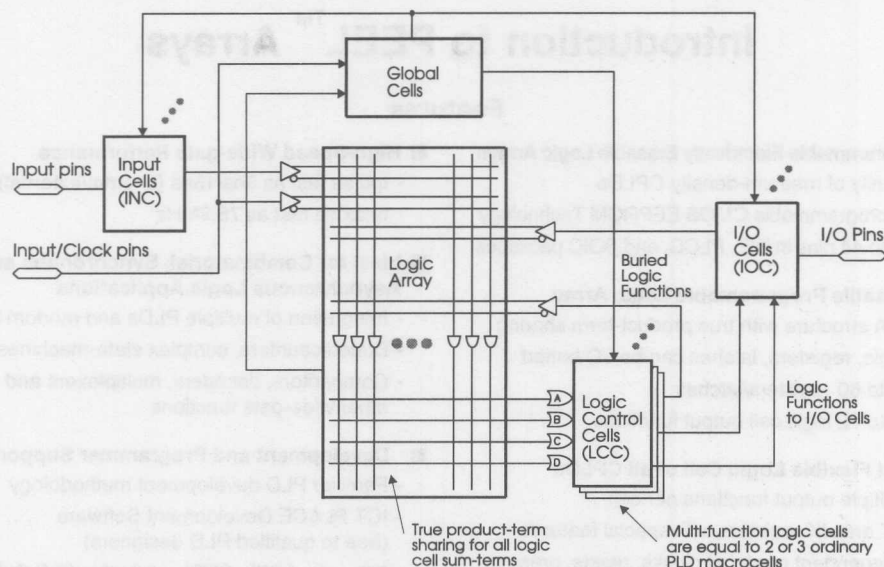


Figure 1. PEEL Array architecture

PEEL Array Architecture Overview

The primary elements of the PEEL Array architecture include I/O cells (IOCs), input cells (INCs), logic control cells (LCCs) and a logic array, as illustrated by the architecture diagram in Figure 1.

Looking at the diagram, input signals to the PEEL Array are first fed through either I/O cells or input cells, each equipped with a user configured register/latch. The signals from the I/O and input cells, as well as feedbacks from the logic control cells, are fed to the logic array with both true and complements available. The logic array, which incorporates a PLA structure with true product term sharing, allows full sum-of-product logic functions to be fed (in groups of four) to each logic control cell.

The logic control cells allocate and control the sum-of-product functions to implement register and I/O cell functions like clocks, sets, presets and output enables as well as combinatorial and sequential output functions. PEEL Array logic cells provide multiple outputs (multi-function) that are equivalent to two or three macrocells of ordinary PLDs. The multiple outputs ensure that registers and logic functions can be buried and that I/Os can still be used for both inputs and outputs. Finally, the global cells allocate global clock signals and other register control functions for logic control cells and I/O cells.

The PEEL Array Family

The PEEL Array family includes three parts in pin-counts ranging from 24 to 44 pins: the PA7024, PA7128 and PA7140. Although the basic architecture is similar, their resources vary relative to the number of inputs, I/Os, logic cells, and array size. The architectural variety of the family efficiently addresses a range of medium-density PLD applications.

The PA7024

Although smallest in pin count of the PEEL Arrays, the PA7024 is by far the most powerful 24-pin PLD today. With 20 I/O pins, 2 inputs/global-clock pins and 40 registers/latches, (20 LCC, 20 IOC) the PA7024 is suitable for a wide variety of applications, see Figure 2. The PA7024's logic array provides 84 sum-of-product functions that share up to 80 product terms. Its multi-function logic cells have two outputs per cell for a total of 40 output functions (20 of which can be buried). To put this in perspective, the popular 22V10 has only 10 non-buried output functions. The PA7024 can implement designs that exceed the architectural capabilities of devices like the 22V10, 20RA10, EP610/630, ATV750, GAL6002, EPM5032. It is also a pin compatible super-set of most any 24-pin PLD. The PA7024 has propagation delays as fast as 10ns/15ns (internal/external) and synchronous clocking frequencies to 71MHz. Power consumption is 120mA max @ 25MHz (85mA typ.). The PA7024 is available in 24-pin DIP, SOIC and 28-pin PLCC packages.

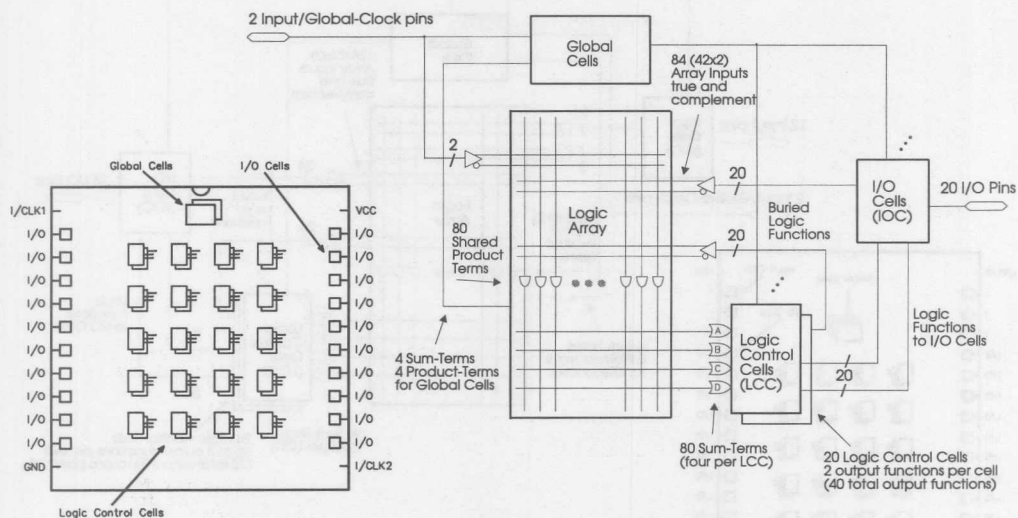


Figure 2. PA7024 block and architecture diagrams

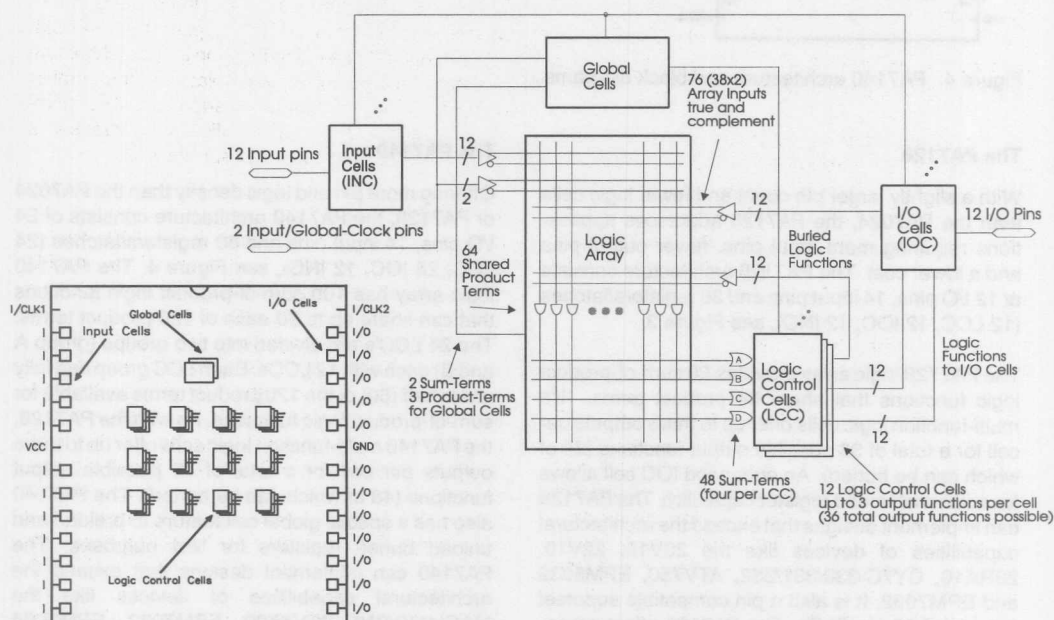


Figure 3. PA7128 block and architecture diagrams

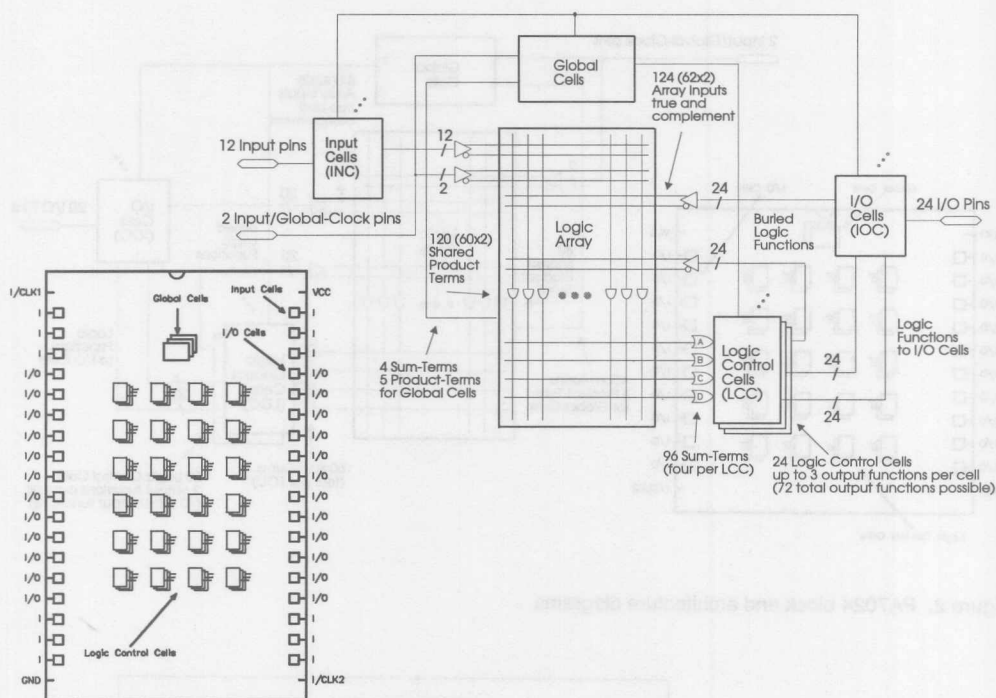


Figure 4. PA7140 architecture and block diagrams

The PA7128

With a slightly larger pin count and fewer logic cells than the PA7024, the PA7128 addresses applications requiring more input pins, fewer output pins and a lower cost. The PA7128 architecture consists of 12 I/O pins, 14 input pins and 36 registers/latches (12 LCC, 12 IOC, 12 INC), see Figure 3.

The PA7128 logic array provides 50 sum-of-product logic functions that share 64 product terms. Its multi-function logic cells offer up to three outputs per cell for a total of 36 possible output functions (24 of which can be buried). An enhanced IOC cell allows for additional buried register capability. The PA7128 can implement designs that exceed the architectural capabilities of devices like the 26V12, 22V10, 20RA10, CY7C-330/331/332, ATV750, EPM5032 and EPM7032. It is also a pin compatible superset to several 28-pin PLDs. The PA7128 offers propagation delays as fast as 9ns/15ns (internal/external) and synchronous clocking frequencies to 83MHz. Power consumption is 105mA max @ 25MHz (75mA typ.). The PA7128 is available in 28-pin DIP, PLCC and SOIC packages.

The PA7140

Offering more pin and logic density than the PA7024 or PA7128, the PA7140 architecture consists of 24 I/O pins, 14 input pins and 60 registers/latches (24 LCC, 24 IOC, 12 INC), see Figure 4. The PA7140 logic array has 100 sum-of-product logic functions that can share up to 60 each of 120 product terms. The 24 LCC's are divided into two groups (group A and B) each with 12 LCCs. Each LCC group can fully share half (60) of the 120 product terms available for sum-of-product logic functions. As with the PA7128, the PA7140 multi-function logic cells offer up to three outputs per cell for a total of 72 possible output functions (48 of which can be buried). The PA7140 also has a special global cell feature to preload and unload buried registers for test purposes. The PA7140 can implement designs that exceed the architectural capabilities of devices like the MACH110/210, ATV2500, EPM7032, EPM5064 and EP910. The PA7140 offers propagation delays as fast as 13ns/20ns (internal/external) and synchronous clocking frequencies to 66MHz. Power consumption is 100mA max @ 25MHz (80mA typ.). The PA7140 is packaged in 40-pin DIP and 44-pin PLCC.

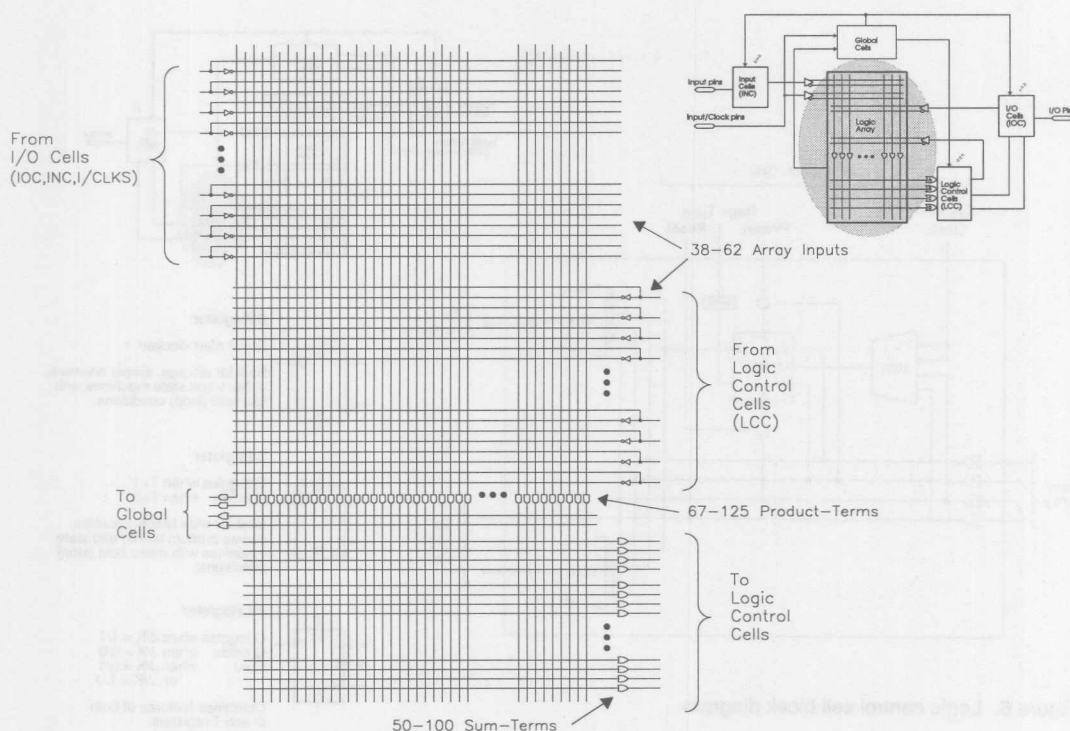


Figure 5. Inside the logic array

A Closer Look at the PEEL Array

Inside the Logic Array

The heart of the PEEL Array architecture is based on a logic array structure similar to that of a PLA (programmable AND, programmable OR). The logic array implements all logic functions and provides interconnection and control of the cells. Depending on the PEEL Array selected, a range of 38 to 62 inputs are available into the array from the I/O cells, inputs cells and input/global-clock pins.

All inputs provide both true and complement signals which can be programmed to any product term in the array. The number of product-terms among PEEL Arrays range from 67 and 125. All product terms (with the exception of certain ones fed to the global cells) can be programmably connected to any of the sum-terms of the logic control cells (four sum-terms per logic control cell). Product-terms and sum-terms are also routed to the global cells for control purposes. Figure 5 shows a detailed view of the logic array structure.

True Product-Term Sharing

The PEEL logic array provides several advantages over common PLD logic arrays. First, it allows for true product-term sharing, not simply product-term steering, as commonly found in other CPLDs. Product term sharing ensures that product-terms are used where they are needed and not left un-utilized or duplicated. Secondly, the sum-of-products functions provided to the logic cells can be used for clocks, resets, presets and output enables instead of just simple product-term control.

The PEEL logic array can also implement logic functions with many product terms within a single-level delay. For example a 16-bit comparator needs 32 shared product terms to implement 16 exclusive-OR functions. The PEEL logic array easily handles this in a single level delay. Other PLDs/CPLDs either run out of product-terms or require expanders or additional logic levels that often slow performance and skew timing.

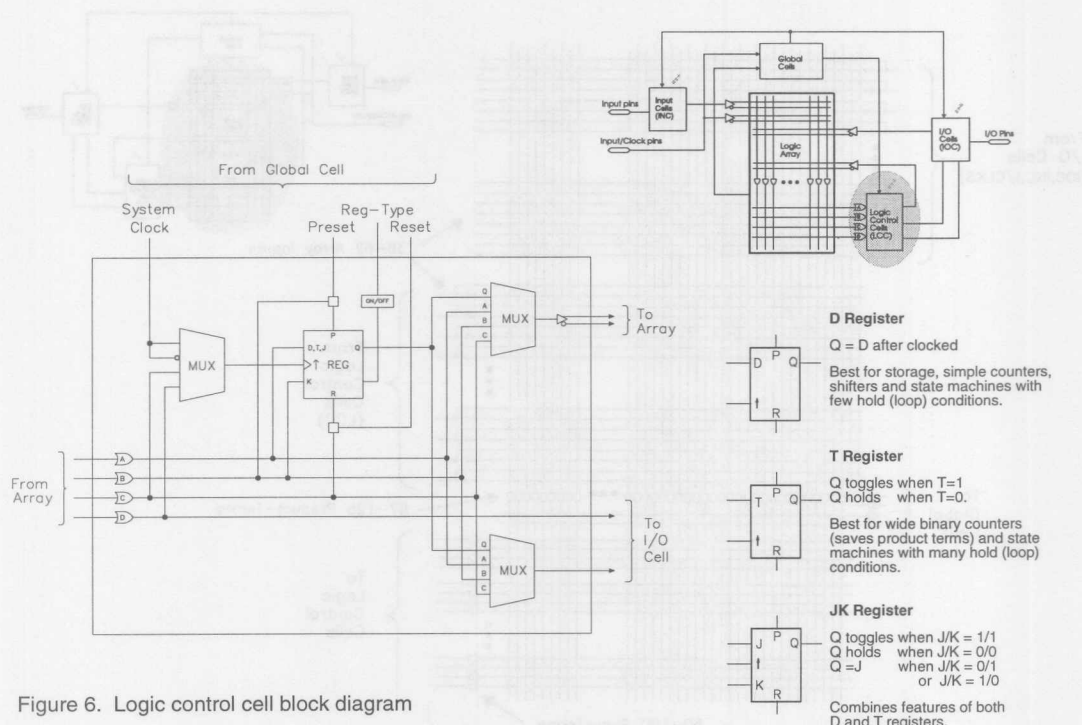


Figure 6. Logic control cell block diagram

Logic Control Cell (LCC)

Logic Control Cells (LCCs) are used to allocate and control the logic functions created in the logic array. Each LCC has four primary inputs and three outputs. The inputs to each LCC are complete sum-of-product logic functions from the array which can be used to implement combinatorial and sequential logic functions, and to control LCC registers and I/O cell output enables.

As shown in Figure 6, the LCC is made up of three signal routing multiplexers and a versatile register with synchronous or asynchronous D, T, or JK registers (clocked-SR registers, which are a subset of JK, are also possible). EEPROM memory cells are used for programming the desired configuration. Four sum-of-product logic functions (SUM terms A, B, C and D) are fed into each LCC from the logic array. Each SUM term can be selectively used for multiple functions as listed below.

Sum-A = D, T, J or Sum-A
 Sum-B = Preset, K or Sum-B
 Sum-C = Reset, Clock, Sum-C
 Sum-D = Clock, Output Enable, Sum-D

SUM-A can serve as the D, T, or J input of the register or a combinatorial path. SUM-B can serve as the K input, or the preset to the register, or a combinatorial path. SUM-C can be the clock, the reset to the register, or a combinatorial path. And, SUM-D can be the clock to the register, the output enable for the connected I/O cell, or an internal feedback node (7128, and 7140 only). Note that the sums controlling clocks, resets, presets and output enables are complete sum-of-product functions, not just product terms as with most other PLDs. This also means that any input or I/O pin can be used as a clock or other control function.

Several signals from the global cell are provided primarily for synchronous (global) register control. The global cell signals are routed to all LCCs. These signals include a high speed clock of positive or negative polarity, global preset and reset, and a special register-type control that selectively allows dynamic switching of register type. This last feature is especially useful for saving product terms when implementing loadable counters and state machines by dynamically switching from D-type registers to load and T-type registers to count (see Figure 9).

Input Cell (INC) for
PA7128, PA7140

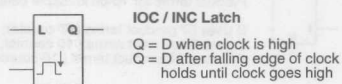
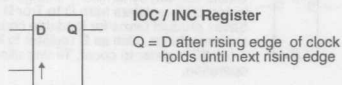
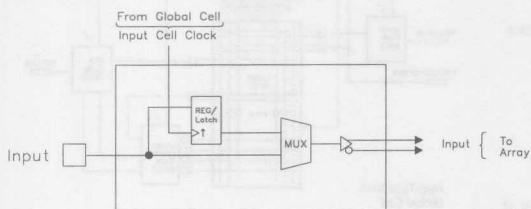


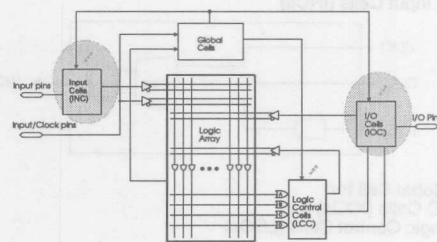
Figure 7. Input Cell (INC) and I/O Cell (IOC) diagrams

Multiple Outputs Per Logic Cell

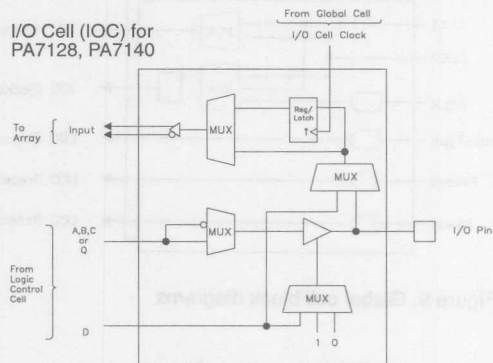
An important feature of the logic control cell is its capability to have multiple output functions per cell each operating independently. As shown in Figure 6, two of the three outputs can select the Q output from the register or the Sum A, B or C combinatorial paths. Thus, one LCC output can be registered, one combinatorial and the third, an output enable, or with the 7128 and 7140, an additional buried logic function. The multi-function PEEL Array logic cells are equivalent to two or three macrocells of other PLDs which have only one output per cell. They also allow registers to be truly buried from I/O pins without limiting them to input-only, (see Figures 7 & 8).

Input Cells (INC)

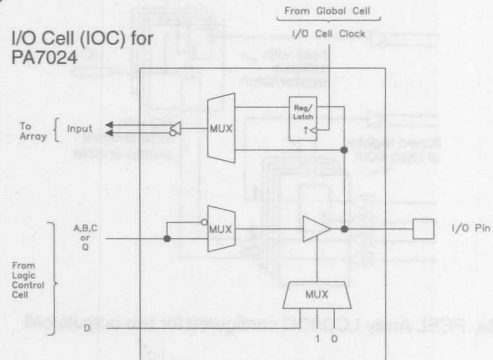
Input cells (INCs) are included with the PA7128 and PA7140 on dedicated input pins. The block diagram of the INC is shown in Figure 7. Each INC consists of a multiplexer and a register/transparent latch which can be clocked from various sources selected by the global cell. The register is rising edge clocked. The latch is transparent when the clock is high and latched on the clock's falling edge. The register/latch can also be bypassed for a non-registered input.



I/O Cell (IOC) for
PA7128, PA7140



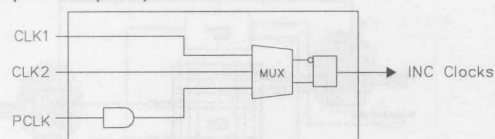
I/O Cell (IOC) for
PA7024



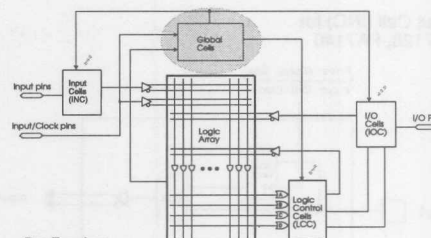
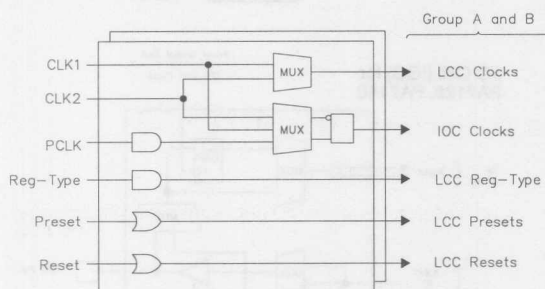
I/O Cell (IOC)

All PEEL Arrays have I/O cells (IOCs) as shown above in Figure 7. Inputs to the IOCs can be fed from any of the LCCs in the array. Each IOC consists of routing and control multiplexers, an input register/transparent latch, a three-state buffer and an output polarity control. The register/latch can be clocked from a variety of sources determined by the global cell. It can also be bypassed for a non-registered input. A feature of the 7128 and 7140 IOC is the use of SUM-D as a feed-back to the array when the I/O pin is a dedicated output. This allows for additional buried registers and logic paths. (See Figures 7 & 8).

Global Cell
for Input Cells (INCs)



Global Cell for
I/O Cells (IOCs) and
Logic Control Cells (LCCs)



Reg-Type from
Global Cell

Register-Type Change Feature

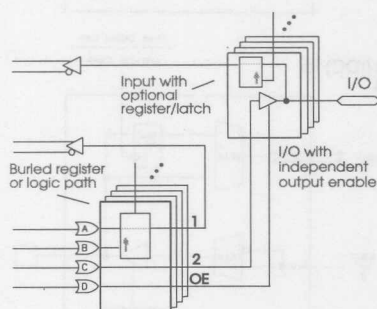
Global cell can dynamically change user-selected LCC registers from D to T or D to JK. Saves product terms for loadable counters and state machines. Use as D register to load, use as T (or JK) register to count. Timing allows dynamic operation.



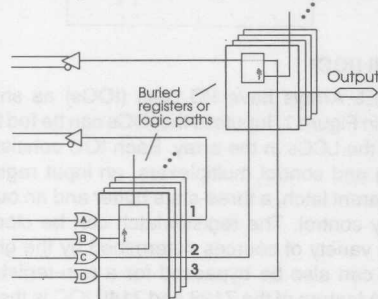
Example:
Product terms for 10-bit loadable binary counter:

D uses 57 product terms (47 counter, 10 load)
T uses 30 product terms (10 counter, 20 load)
D/T uses 20 product terms (10 counter, 10 load)

Figure 9. Global cell block diagrams



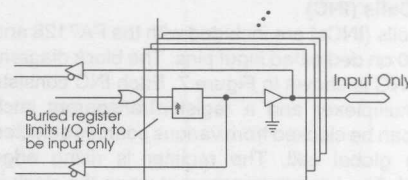
8a. PEEL Array LCC/IOC configured for two outputs/cell



8b. PEEL Array LCC/IOC configured for three outputs/cell

Global Cells

The global cells, shown in Figure 9, are used to direct global clock signals and/or control terms to the LCCs, IOCs and INCs. The global cells allow a clock to be selected from the CLK1 pin, CLK2 pin, or a product term from the logic array (PCLK). They also provide polarity control for INC and IOC clocks enabling rising or falling clock edges for input registers/latches. Note that each individual LCC clock has its own polarity control. The global cell for LCCs includes sum-of-products control terms for global reset and preset, and a fast product term control for LCC register-type, used to save product terms for loadable counters and state machines (see Figure 8). If additional flexibility is needed, the PA7024 and PA7140 provide a second global cell that divides the LCC and IOCs into two groups, A and B. Half of the LCCs and IOCs use global cell A, half use global cell B. This means, for instance, two high speed global clocks can be used among the LCCs.



8c. Other PLDs with only one output per I/O macrocell

Figure 8a-c: PEEL Array multiple outputs/cell allow buried registers without limiting I/O to input only

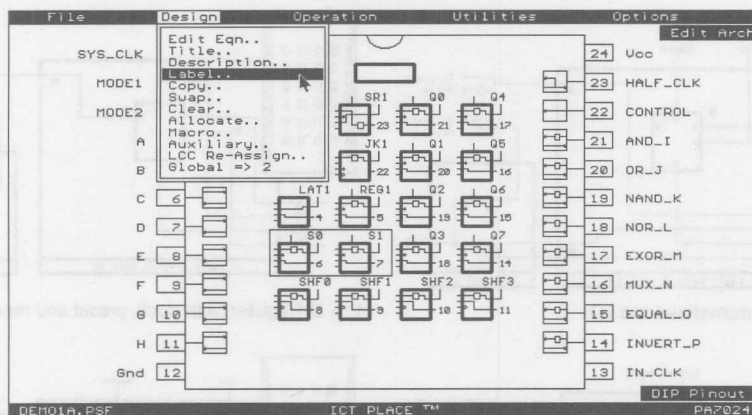


Figure 10a. PLACE Architectural Editor for PA7024

PEEL Array Development Support

Development support for PEEL Arrays is provided by ICT and manufacturers of popular development tools. ICT offers the powerful PLACE Development Software (free to qualified PLD designers).

The PLACE software includes an architectural editor, logic compiler, waveform simulator, documentation utility and a programmer interface. The PLACE editor graphically illustrates and controls the PEEL Array's architecture, making the overall design easy to understand, while allowing the effectiveness of boolean logic equations, state machine design and truth table entry. The PLACE compiler performs logic transformation and reduction making it possible to specify equations in most any fashion and fit the most logic possible in every design. PLACE also provides a multi-level logic simulator allowing external and internal signals to be simulated and analyzed via a waveform display. (See Figures 10a-c.)

PEEL Array development is also supported by popular development tools, such as ABEL and CUPL, via ICT's PEEL Array fitters. A special smart translator utility adds the capability to directly convert JEDEC files for other devices into equivalent JEDEC files for pin-compatible PEEL Arrays.

Programming

PEEL Arrays are EE-reprogrammable in all package types, plastic-DIP, PLCC and SOIC. This makes them an ideal development vehicle for the lab. EE-reprogrammability is also useful for production, allowing unexpected changes to be made quickly and without waste. Programming of PEEL Arrays is supported by ICT's PDS-series programmers, as well as many other popular third party programmers.

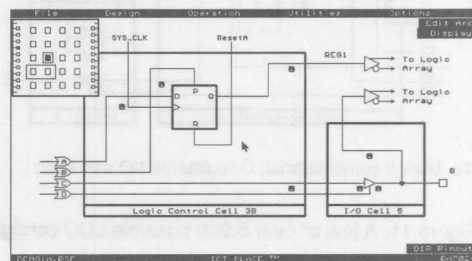


Figure 10b. PLACE LCC and IOC screen

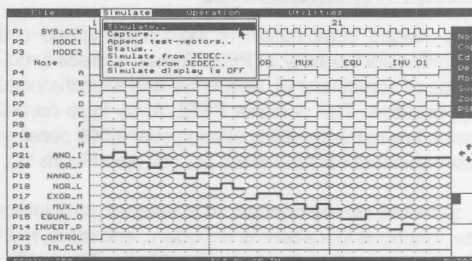
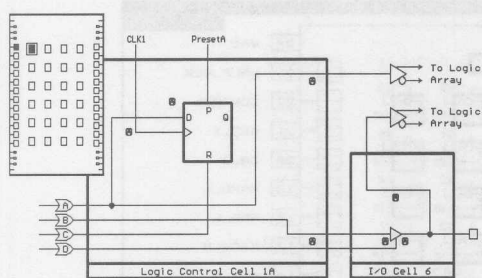


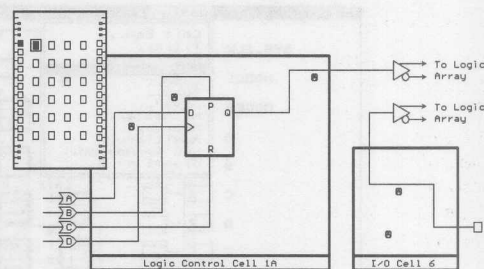
Figure 10c. PLACE waveform simulator screen

Design Security and Signature Word

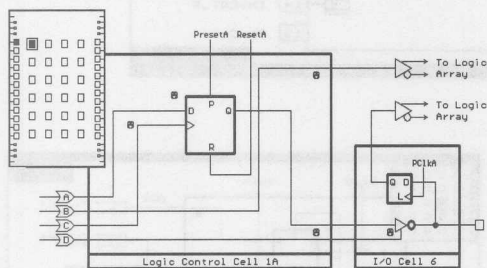
The PEEL Arrays provide a special EEPROM security bit that prevents unauthorized reading or copying of designs. Once set, the programmed bits of the PEEL Arrays cannot be accessed until the entire chip has been electrically erased. Another programming feature, signature word, allows a user-definable code to be programmed into the PEEL Array. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed in the device or to record the design revision.



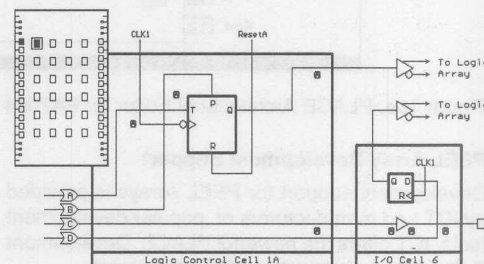
11a. Buried combinational and I/O



11b. D-Register (with clock, preset and reset) and input



11c. Buried combinational, D-registered I/O with latch



11d. 3 functions: buried T-reg., buried D-reg., and output

Figure 11. A few of over 8,000 possible LCC configurations

PEEL Array Applications

The unique combination of logic array speed and architectural flexibility let PEEL Arrays address a multitude of combinational, sequential and asynchronous applications. The versatile PEEL Array logic control cell is key to this flexibility offering over 8,000 possible user-selected configurations per cell (see Figure 11).

Logic cells can be configured to support combinational functions like address decoders, encoders, multiplexers, comparators, and adders. They also handle asynchronous random logic such as D flip-flops (i.e., 7474) with independent clock reset and preset, SR latches and gated latches. Additionally, synchronous registered functions, like shifters, clock dividers, counters, and state machines are

possible. Because PEEL Array registers have multiple outputs, buried counters and state machines with decode are easily supported (see Figure 12).

Input latches add further flexibility allowing pipelined operation, direct demultiplexing and gated-strobing of address/data lines. Additionally, the number of registers and latches available for data storage, as well as tri-state I/Os, open many possibilities for bus interfaced sub-systems.

For more information on PEEL Array applications examples please refer to the PLACE Users Manual and the example design files provided with the PLACE software.

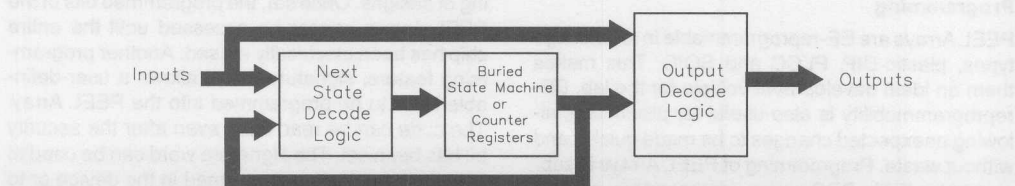


Figure 12. Buried counters and state machines

Why PEEL Arrays are Unique to Other CPLDs

The PEEL Array architecture combines a non-segmented programmable logic array (PLA) with FPGA-style logic cells that free PLD users from the architectural restrictions of simple PALs/GALs and the PAL-like blocks of segmented CPLDs. They are also rich in buried registers/latches and logic functions (see Table 1). Key PEEL Array architectural features include:

Complete Input/Feedback Availability.

Every input pin and feedback is available for use by any logic function. As a result PEEL Array input availability is two to three times that of segmented CPLD blocks, guaranteeing connectivity for wide-gate logic in single level delays as well as flexible I/O assignment.

Real Product Term Sharing via a Wide-gate PLA.

The PEEL Array non-segmented PLA allows real product term sharing for wide-gate functions like comparitors and state-machines. Over 60 product terms are available per function as compared to segmented CPLDs which have a limited number of product terms per function supplemented by term steering or expander schemes that can limit logic utilization or adversely affect timing.

True I/O buried registers via FPGA-style logic cells.

PEEL Array logic cells have multiple functions per cell, similar to FPGAs and equal to 2-3 ordinary PLD macrocells. Thus, registers (or combinatorial logic functions) can be buried from I/O pins without sacrificing the output functions of I/Os as many CPLD macrocells do.

Flexible Registers with independent clocks and sum-of-products control.

PEEL Arrays have D,T and JK registers that allow clocks, presets and resets to be individually or globally controlled via full sum-of-product functions from the PLA. Some segmented CPLDs share register clocks, presets and resets via single product terms.

Independent Output Enables with sum-of-products control.

PEEL Arrays allow for complex output enables with individual sum-of-products control instead of dedicated pins or single product terms as used by most segmented CPLDs.

For more information on PEEL Arrays and other ICT products contact ICT Inc. at 1-800-SAY-PEEL x322. (1-800-729-7335 x322).

Architecture Specification	PA7024	PA7128	PA7140
Pin Count	24 / 28	28	40 / 44
Package Types	DIP, SOIC / PLCC	DIP, SOIC, PLCC	DIP / PLCC
Total PLA Inputs/Feedbacks (true and complement)	84 (42 x 2)	76 (38 x 2)	124 (62 x 2)
Inputs	2	14	14
I/Os	20	12	24
Buriable Feedbacks	20	24	48
Logic Control Cells	20 Dual Function	12 Triple Function	24 Triple Function
Logic Functions	40 (20 buried, 20 output)	36 (24 buried, 12 output)	72 (48 buried, 24 output)
Total Product Terms	84	67	125
Product terms per I/O	80	64	60
Total Sum Terms	84	50	100
Total Registers/Latches	40	36	60
Buriable Registers	20	24	48
Input Reg/Latches	20	24	36

Table 1. PEEL Array family architecture specifications



PEEL Array Functional Cross Reference

V1.0

Altera	ICT Pin Compatible ¹	ICT Superset /Alternative
EP600	PA7024	PA7128 ²
EP610	PA7024	PA7128 ²
EP900	PA7140	PA7128 ³
EP910	PA7140	PA7128 ³
EP1800	-	PA7140 ³
EP1810	-	PA7140 ³
EPM5032	-	PA7128 ⁴
EPS464	-	PA7140 ⁴
EPM5064	-	PA7140 ⁴
EPM7032	-	PA7128 ³ , 7140 ⁵
AMD		
PALCE24V10	PA7128	-
PALCE26V12	PA7128	-
PALCE29M16	PA7024	PA7128 ²
PALCE29MA16	PA7024	PA7128 ²
PALCE610	PA7024	PA7128 ²
PALCE20RA10	PA7024	PA7128 ²
MACH110-15	-	PA7128 ⁶
		PA7140 ⁵
MACH210-20	-	PA7140 ⁴
Atmel		
ATV750	PA7024	PA7128 ²
ATV2500	-	PA7140 ⁵
ATH3000	-	PA7140 ⁶
Cypress		
PLDC20RA10	PA7024	PA7128 ²
CG7C324	PA7024	PA7128 ²
CY7C330	-	PA7128 ⁵
CY7C331	-	PA7128 ⁵
CY7C332	-	PA7128 ⁵
CY7C335	-	PA7128 ⁵
CY7C343	-	PA7140 ⁴
CY7C344	-	PA7128 ⁴
CY7C371	-	PA7140 ⁵
		PA7128 ⁶
CY7C372	-	PA7140 ⁴
Intel		
PLD610	PA7024	PA7128 ²
PLD910	PA7140	PA7128 ³
5C060	PA7024	PA7128 ²
5C090	PA7140	PA7128 ³
5C180	-	PA7140 ³
5AC312	PA7024	PA7128 ²
5AC324	-	PA7140 ⁵
44FX740	-	PA7140 ⁵

Lattice		
GAL20RA10	PA7024	PA7128 ²
GAL20XV10B	PA7024	PA7128 ²
GAL26CV12B	PA7128	-
GAL6001B	PA7024	PA7128 ²
GAL6002B	PA7024	PA7128 ²
pLSI 1016	-	PA7140 ⁴
ispLSI 1016	-	PA7140 ⁴
pLSI 2032	-	PA7140 ⁵
ispLSI 2032	-	PA7140 ⁵
National		
GAL20RA10	PA7024	PA7128 ²
GAL6001	PA7024	PA7128 ²
MAPL128	-	PA7128 ⁴
MAPL144	-	PA7140 ⁵
MAPL244	-	PA7140 ⁴
Philips		
PLS100	-	PA7128 ⁵
PLS173/B	PA7024	PA7128 ²
PLS105/A	-	PA7128 ⁵
PLUS405	-	PA7128 ⁵
PLS167/A	-	PA7024 ⁵
		PA7128 ²
PLS168/A	-	PA7024 ⁵
		PA7128 ²
PLS179	PA7024	PA7128 ²
PLC42VA12	PA7024	PA7128 ²
PLC415	-	PA7128 ⁵
PLHS501	-	PA7140 ³
PML2552	-	PA7140 ³
TI		
EP630	PA7024	PA7128 ²
EP1830	-	PA7140 ³
Xilinx		
XC7236/A	-	PA7140 ⁵
		PA7128 ⁶
XC7336	-	PA7140 ⁵
		PA7128 ⁶
XC7354	-	PA7140 ⁴

- 1) Pin-compatible PEEL Arrays nearly always provide a higher logic capacity than the devices they replace.
- 2) These devices have more pins and higher logic capacity than the devices they replace.
- 3) These devices have less pins but higher logic capacity than the devices they replace.
- 4) These devices, though not pin compatible, have the same number of pins and approximately the same logic capacity as the devices they replace.
- 5) These devices, though not pin compatible, have the same number of pins and higher logic capacity than the devices they replace.
- 6) These devices have fewer pins but approximately the same logic capacity as the devices they replace.

PA7024 PEEL™ Array Programmable Electrically Erasable Logic Array

2

Features

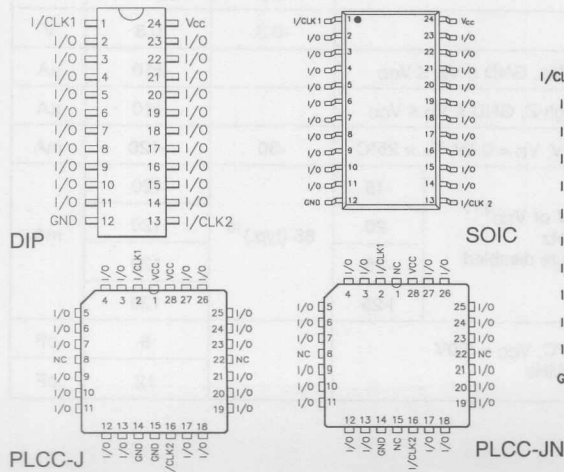
- **CMOS Electrically Erasable Technology**
 - Reprogrammable in 24-pin DIP, SOIC, and 28-pin PLCC packages
- **Most Powerful 24-pin PLD Available**
 - 20 I/Os, 2 inputs/clocks, 40 registers/latches
 - 40 logic cell output functions
 - PLA structure with true product-term sharing
 - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
 - Multiple output functions per cell
 - D,T and JK registers with special features
 - Independent or global clocks, resets, presets, clock polarity, and output enables
 - Sum-of-products logic for output enables
- **High-Speed Commercial and Industrial Versions**
 - As fast as 10ns/15ns (tpdi/tpdx), 71.4MHz fmax
 - Industrial grade available for 4.5 to 5.5V Vcc and -40 to +85°C temperatures
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
 - Integration of multiple PLDs and random logic
 - Buried counters, complex state-machines
 - Comparitors, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
 - ICT PLACE Development Software
 - Fitters for ABEL, CUPL and other software
 - Programming support by ICT PDS-3 and popular third-party programmers

General Description

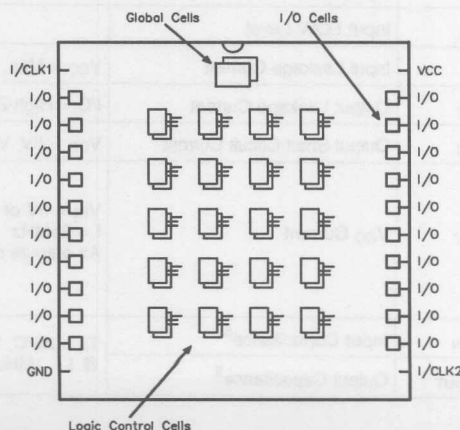
The PA7024 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7024 is by far the most powerful 24-pin PLD available today with 20 I/O pins, 2 input/global-clocks and 40 registers/latches (20 buried logic cells and 20 I/O reg/latches). Its logic array implements 84 sum-of-product logic functions that share 80 product terms. The PA7024's logic and I/O cells (LCCs, IOCs) are extremely flexible, offering two output functions per logic cell (a total of 40 for all 20 logic cells). Logic cells are configurable as D,

T and JK registers with independent or global clocks, resets, presets, clock polarity and other special features, making them suitable for a wide variety of combinatorial, synchronous and asynchronous logic applications. With pin compatibility and super-set functionality to most 24-pin PLDs, (22V10, EP610/630, GAL6002), the PA7024 can implement designs that exceed the architectures of such devices. The PA7024 supports speeds as fast as 10ns/15ns (tpdi/tpdx) and 71.4MHz (fmax) at moderate power consumption 120mA (85mA typical). Packaging includes 24-pin DIP, SOIC and 28-pin PLCC. Development and programming support for the PA7024 is provided by ICT and popular third-party development tool manufacturers.

Pin Configurations



Block Diagram



This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T _A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T _R	Clock Rise Time	See Note 2		20	ns
T _F	Clock Fall Time	See Note 2		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 2		250	ms

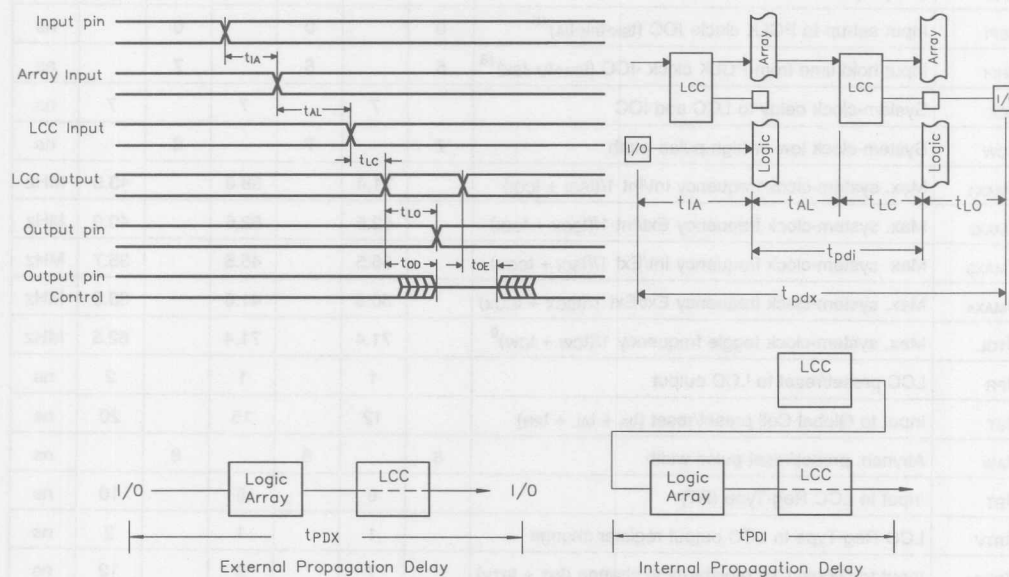
D.C. Electrical Characteristics Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage - CMOS	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{OLc}	Output LOW Voltage - CMOS	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		-0.3	0.8	V
I _{IL}	Input Leakage Current	V _{CC} = Max, GND ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V _O ≤ V _{CC}		±10	μA
I _{SC}	Output Short Circuit Current ⁴	V _{CC} = 5V, V _O = 0.5V, T _A = 25°C	-30	-120	mA
I _{CC}	V _{CC} Current	V _{IN} = 0V or V _{CC} ^{3,11} f = 25MHz All outputs disabled	-15	120	mA
			-20	120	
			-25	120	
			I-25	130	
C _{IN}	Input Capacitance ⁵	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT}	Output Capacitance ⁵			12	pF

A.C. Electrical Characteristics Combinatorial

Over the Operating Range

Symbol	Parameter ^{6,12}	-15		-20 ¹⁷		-25 / I-25 ¹⁷		Unit
		Min	Max	Min	Max	Min	Max	
t _{PDI}	Propagation delay Internal (t _{AL} + t _{LC})		10		13		17	ns
t _{PDX}	Propagation delay External (t _{IA} + t _{AL} + t _{LC} + t _{LO})		15		20		25	ns
t _{IA}	Input or I/O pin to Array input		2		2		2	ns
t _{AL}	Array input to LCC		9		12		16	ns
t _{LC}	LCC input to LCC output ¹⁰		1		1		1	ns
t _{LO}	LCC output to output pin		3		5		6	ns
t _{OD} , t _{OE}	Output Disable, Enable from LCC output ⁷		3		5		6	ns
t _{OX}	Output Disable, Enable from input pin ⁷		15		20		25	ns

Combinatorial Timing - Waveforms and Block Diagram


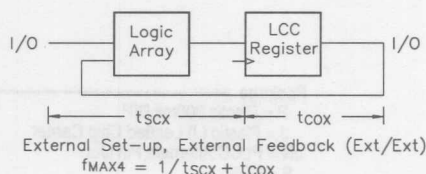
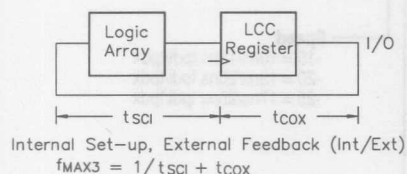
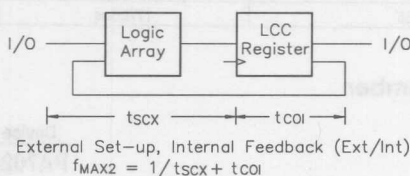
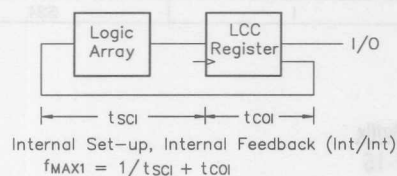
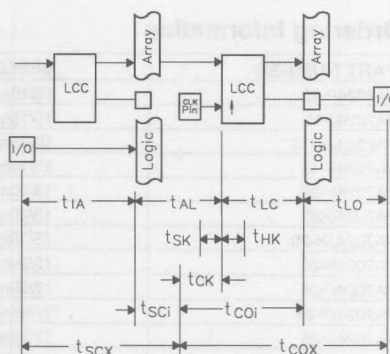
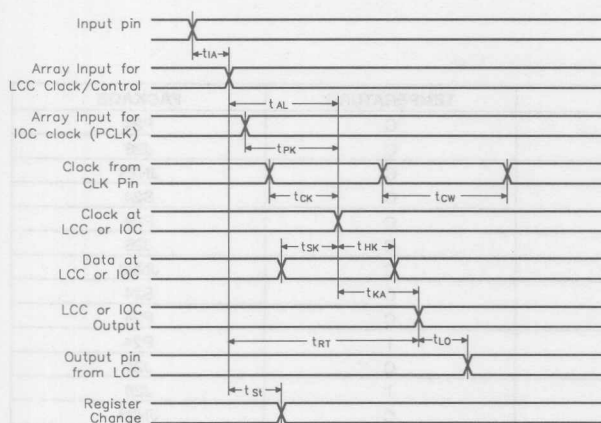
A.C. Electrical Characteristics Sequential

Over the Operating Range

Symbol	Parameter ^{6,12}	-15		-20 ¹⁷		-25 / I-25 ¹⁷		Unit
		Min	Max	Min	Max	Min	Max	
tSCI	Internal set-up to system-clock ⁸ - LCC ¹⁴ (tAL + tSK + tLC - tCK)	6		9		15		ns
tSCX	Input ¹⁵ (Ext.) set-up to system clock, -LCC (tIA + tSCI)	8		11		17		ns
tCOI	System-clock to Array Int. -LCC/IOC ¹⁴ (tCK + tLC)		8		8		8	ns
tCOX	System-clock to Output Ext. - LCC (tCOI + tLO)		12		13		13	ns
tHX	Input hold time from system clock - LCC	0		0		0		ns
tSK	LCC input set-up to async. clock ¹³ - LCC	3		3		4		ns
tAK	Clock at LCC or IOC - LCC output	1		1		1		ns
tHK	LCC input hold time from async. clock - LCC	4		4		4		ns
tSI	Input set-up to system clock - IOC ¹⁴ (tSK - tCK)	0		0		0		ns
tHI	Input hold time from system clock - IOC (tCK - tSK)	4		4		4 / 3		ns
tpK	Array input to IOC PCLK clock		6		7		9	ns
tSPI	Input set-up to PCLK clock- IOC (tSK-tpK-tIA) ¹⁶	0		0		0		ns
tHPI	Input hold time from PCLK clock -IOC (tpK+tIA-tSK) ¹⁶	5		6		7		ns
tCK	System-clock delay to LCC and IOC		7		7		7	ns
tCW	System-clock low or high pulse width	7		7		8		ns
fMAX1	Max. system-clock frequency Int/Int 1/(tSCI + tCOI)		71.4		58.8		43.5	MHz
fMAX2	Max. system-clock frequency Ext/Int 1/(tSCX + tCOI)		62.5		52.6		40.0	MHz
fMAX3	Max. system-clock frequency Int/Ext 1/(tSCI + tCOX)		55.5		45.5		35.7	MHz
fMAX4	Max. system-clock frequency Ext/Ext 1/(tSCX + tCOX)		50.0		41.6		33.3	MHz
fTGL	Max. system-clock toggle frequency 1/(tcw + tcw) ⁹		71.4		71.4		62.5	MHz
tPR	LCC preset/reset to LCC output		1		1		2	ns
tST	Input to Global Cell preset/reset (tIA + tAL + tPR)		12		15		20	ns
tAW	Asynch. preset/reset pulse width	8		8		8		ns
tRT	Input to LCC Reg-Type (RT)		6		8		10	ns
tRTV	LCC Reg-Type to LCC output register change		1		1		2	ns
tRTC	Input to Global Cell register-type change (tRT + tRTV)		7		9		12	ns
tRW	Asynch. Reg-Type pulse width	10		10		10		ns
tRESET	Power-on reset time for registers in clear state ²		5		5		5	μs

Sequential Timing - Waveforms and Block Diagram

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Notes:

- Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
- Test points for Clock and V_{CC} in t_R , t_F , t_{CL} , t_{CH} , and t_{RESET} are referenced at 10% and 90% levels.
- I/O pins are 0V or V_{CC} .
- Test one output at a time for a duration of less than 1 sec.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$ (See test loads for V_{REF} value).
 t_{OD} is measured from input transition to $VOH - 0.1V$ or $VOL + 0.1V$.
- "System-clock" refers to pin 1 or 13 (2 or 16 PLCC) high speed clocks.
- For T or JK registers in toggle (divide by 2) operation only.
- For combinatorial and async-clock to LCC output delay.
- lcc for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
- Test loads are specified in Section 6 of this Data Book.
- "Async. clock" refers to the clock from the Sum term (OR gate).
- The "LCC" term indicates that the timing parameter is applied to the LCC register. The "IOC" term indicates that the timing parameter is applied to the IOC register. The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and IOC registers.
- The term "Input" without any reference to another term refers to an (external) input pin.
- The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of $(t_{SK} - t_{PK} - t_{IA})$. This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
- PA7024-1 is an alternate number for PA7024-20. PA7024-2 is an alternate number for PA7024-25.
- Typical (typ) lcc is measured at $T_A = 25^\circ C$, Freq = 25MHz, $V_{CC} = 5V$.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PA7024P-15	10/15ns	C	P24
PA7024J-15	10/15ns	C	J28
PA7024JN-15	10/15ns	C	JN28
PA7024S-15	10/15ns	C	S24
PA7024P-20	13/20ns	C	P24
PA7024J-20	13/20ns	C	J28
PA7024JN-20	13/20ns	C	JN28
PA7024S-20	13/20ns	C	S24
PA7024P-25	17/25ns	C	P24
PA7024PI-25	17/25ns	I	P24
PA7024J-25	17/25ns	C	J28
PA7024JI-25	17/25ns	I	J28
PA7024JN-25	17/25ns	C	JN28
PA7024S-25	17/25ns	C	S24
PA7024SI-25	17/25ns	I	S24

Part Number

Device Suffix
PA7024P-15

Package

P = Plastic 300mil DIP
 J = Plastic (J) Leaded Chip Carrier
 JN = PLCC Alternate Pin Out
 S = SOIC

Speed

-15 = 10ns/15ns tpd/tpdx
 -20 = 13ns/20ns tpd/tpdx
 -25 = 17ns/25ns tpd/tpdx

Temperature Range

(Blank) = Commercial 0 to +70°C
 I = Industrial -40 to +85°C

PA7128 PEEL™ Array **Programmable Electrically Erasable Logic Array**

2

Features

■ CMOS Electrically Erasable Technology

- Reprogrammable in 28-pin DIP, SOIC, and PLCC packages

■ Versatile Logic Array Architecture

- 12 I/Os, 14 inputs, 36 registers/latches
- Up to 36 logic cell output functions
- PLA structure with true product-term sharing
- Logic functions and registers can be I/O-buried

■ Flexible Logic Cell

- Up to 3 output functions per logic cell
- D, T and JK registers with special features
- Independent or global clocks, resets, presets, clock polarity, and output enables
- Sum-of-products logic for output enables

■ High-Speed Commercial and Industrial Versions

- As fast as 9ns/15ns (tpdi/tpdx), 83.3MHz fmax
- Industrial grade available for 4.5 to 5.5V Vcc and -40 to +85 °C temperatures

■ Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications

- Integration of multiple PLDs and random logic
- Buried counters, complex state-machines
- Comparators, decoders, other wide-gate functions

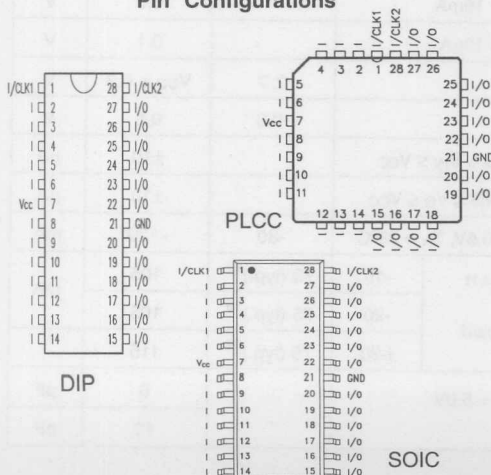
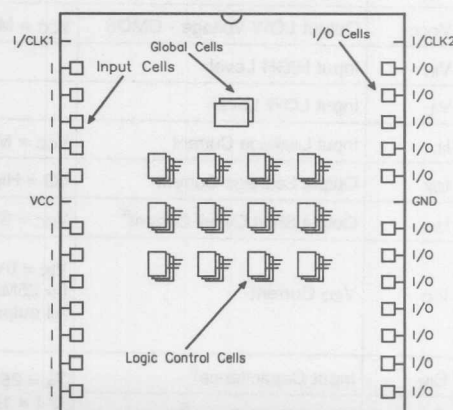
■ Development and Programmer Support

- ICT PLACE Development Software
- Fitters for ABEL, CUPL and other software
- Programming support by ICT PDS-3 and other popular third-party programmers

General Description

The PA7128 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's 1-micron CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7128 offers a versatile logic array architecture with 12 I/O pins, 14 input pins and 36 registers/latches (12 buried logic cells, 12 input reg/latches, 12 buried I/O reg/latches). Its logic array implements 50 sum-of-product functions that share 64 product terms. The PA7128's logic and I/O cells (LCCs, IOCs) are extremely flexible offering up to three output functions per cell (a total of 36 for all 12 logic cells). Cells are

configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity and other special features, making the PA7128 suitable for a variety of combinatorial, synchronous and asynchronous logic applications. The PA7128 offers pin compatibility and super-set functionality to popular 28-pin PLDs, like the 26V12. Thus, designs that exceed the architectures of such devices can be expanded upon. The PA7128 supports speeds as fast as 9ns/15ns (tpdi/tpdx) and 83.3MHz (fmax) at moderate power consumption 105mA (75mA typical). Packaging includes 28-pin DIP, SOIC and PLCC. Development and programming support for the PA7128 is provided by ICT and popular third party development tool manufacturers.

Pin Configurations

Block Diagram


This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T _A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T _R	Clock Rise Time	See Note 2		20	ns
T _F	Clock Fall Time	See Note 2		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 2		250	ms

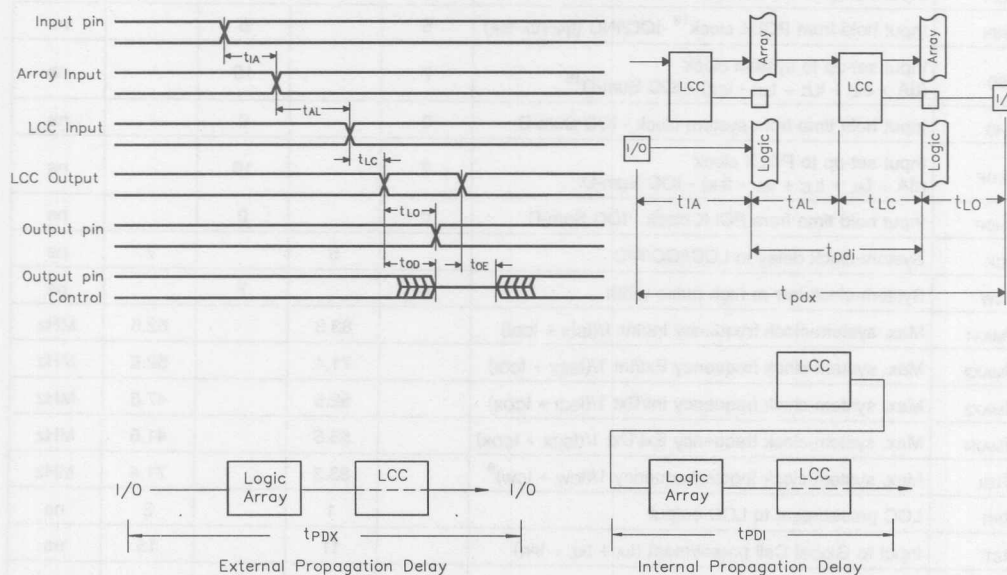
D.C. Electrical Characteristics Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage - CMOS	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{OLc}	Output LOW Voltage - CMOS	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		-0.3	0.8	V
I _{IL}	Input Leakage Current	V _{CC} = Max, GND ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V _O ≤ V _{CC}		±10	μA
I _{SC}	Output Short Circuit Current ⁴	V _{CC} = 5V, V _O = 0.5V, T _A = 25°C	-30	-120	mA
I _{CC}	V _{CC} Current	V _{IN} = 0V or V _{CC} ^{3,11} f = 25MHz All outputs disabled	-15	75 (typ.) ¹⁹	mA
			-20	75 (typ.) ¹⁹	
			-1-20	75 (typ.) ¹⁹	
C _{IN}	Input Capacitance ⁵	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT}	Output Capacitance ⁵			12	pF

A.C. Electrical Characteristics Combinatorial

Over the Operating Range

Symbol	Parameter ^{6, 12}	-15 ¹⁷		-20 / I-20 ¹⁷		Unit
		Min	Max	Min	Max	
t _{PDI}	Propagation delay Internal (t _{AL} + t _{LC})		9		12	ns
t _{PDX}	Propagation delay External (t _{IA} + t _{AL} + t _{LC} + t _{LO})		15		20	ns
t _{IA}	Input or I/O pin to Array input		2		3	ns
t _{AL}	Array input to LCC		8		10	ns
t _{LC}	LCC input to LCC output ¹⁰		1		2	ns
t _{LO}	LCC output to output pin		4		5	ns
t _{OD} , t _{OE}	Output Disable, Enable from LCC output ⁷		4		5	ns
t _{OX}	Output Disable, Enable from input pin ⁷		15		20	ns

Combinatorial Timing - Waveforms and Block Diagram


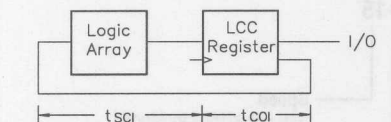
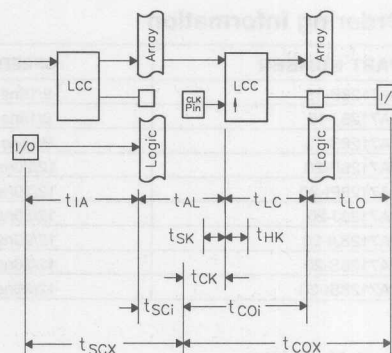
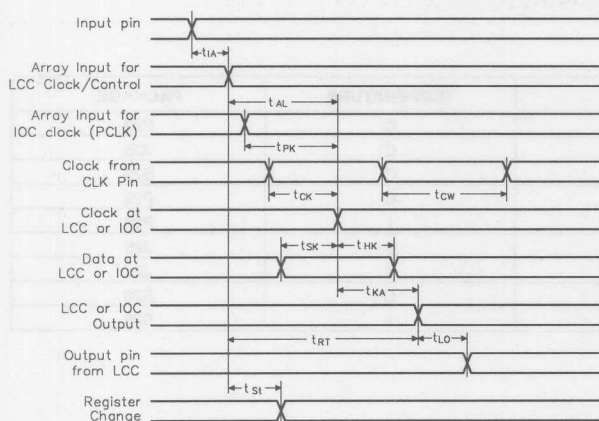
A.C. Electrical Characteristics Sequential

Over the Operating Range

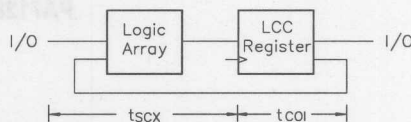
Symbol	Parameter ^{6, 12}	-15 ¹⁷		-20 / I-20 ¹⁷		Unit
		Min	Max	Min	Max	
tSCI	Internal set-up to system-clock ⁸ - LCC ¹⁴ (tAL + tSK + tLC - tCK)	5		7		ns
tSCX	Input ¹⁶ (Ext.) set-up to system clock, -LCC (tIA + tSCI)	7		10		ns
tCOI	System-clock to Array Int. -LCC/IOC/INC ¹⁴ (tCK + tLC)		7		9	ns
tCOX	System-clock to Output Ext. - LCC (tCOI + tLO)		11		14	ns
tHX	Input hold time from system clock - LCC	0		0		ns
tSK	LCC input set-up to async. clock ¹³ - LCC	2		2		ns
tAK	Clock at LCC or IOC - LCC output	1		1		ns
tHK	LCC input hold time from async. clock - LCC	4		4		ns
tSI	Input set-up to system clock - IOC/INC ¹⁴ (tSK - tCK)	0		0		ns
tHI	Input hold time from system clock - IOC/INC (tCK - tSK)	4		5		ns
tPK	Array input to IOC PCLK clock		6		7	ns
tSPI	Input set-up to PCLK clock ¹⁸ - IOC/INC (tSK - tPK - tIA)	0		0		ns
tHPI	Input hold from PCLK clock ¹⁸ - IOC/INC (tPK + tIA - tSK)	6		8		ns
tSD	Input set-up to system clock (tIA + tAL + tLC + tSK - tCK) - IOC Sum-D ¹⁵	7		10		ns
tHD	Input hold time from system clock - IOC Sum-D	0		0		ns
tSDP	Input set-up to PCLK clock (tIA + tAL + tLC + tSK - tPK) - IOC Sum-D	7		10		ns
tHDP	Input hold time from PCLK clock - IOC Sum-D	0		0		ns
tCK	System-clock delay to LCC/IOC/INC		6		7	ns
tCW	System-clock low or high pulse width	6		7		ns
fMAX1	Max. system-clock frequency Int/Int 1/(tSCI + tCOI)		83.3		62.5	MHz
fMAX2	Max. system-clock frequency Ext/Int 1/(tSCX + tCOI)		71.4		52.6	MHz
fMAX3	Max. system-clock frequency Int/Ext 1/(tSCI + tCOX)		62.5		47.6	MHz
fMAX4	Max. system-clock frequency Ext/Ext 1/(tSCX + tCOX)		55.5		41.6	MHz
fTGL	Max. system-clock toggle frequency 1/(tCW + tCW) ⁹		83.3		71.4	MHz
tPR	LCC preset/reset to LCC output		1		2	ns
tST	Input to Global Cell preset/reset (tIA + tAL + tPR)		11		15	ns
tAW	Asynch. preset/reset pulse width	8		8		ns
tRT	Input to LCC Reg-Type (RT)		7		9	ns
tRTV	LCC Reg-Type to LCC output register change		1		2	ns
tRTC	Input to Global Cell register-type change (tRT + tRTV)		8		11	ns
tRW	Asynch. Reg-Type pulse width	10		10		ns
tRESET	Power-on reset time for registers in clear state ²		5		5	μs

Sequential Timing - Waveforms and Block Diagram

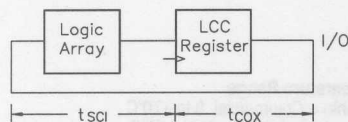
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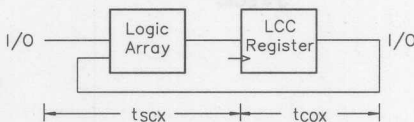
Internal Set-up, Internal Feedback (Int/Int)
 $f_{MAX1} = 1/t_{SCI} + t_{COI}$



External Set-up, Internal Feedback (Ext/Int)
 $f_{MAX2} = 1/t_{SCX} + t_{COI}$



Internal Set-up, External Feedback (Int/Ext)
 $f_{MAX3} = 1/t_{SCI} + t_{COX}$



External Set-up, External Feedback (Ext/Ext)
 $f_{MAX4} = 1/t_{SCX} + t_{COX}$

Notes:

- Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
- Test points for Clock and V_{CC} in t_R , t_F , t_{CL} , t_{CH} , and t_{SET} are referenced at 10% and 90% levels.
- I/O pins are 0V or V_{CC} .
- Test one output at a time for a duration of less than 1 sec.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$ (See test loads at end of Section 6 for V_{REF} value).
- t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
- "System-clock" refers to pin 1 or pin 28 high speed clocks.
- For T or JK registers in toggle (divide by 2) operation only.
- For combinatorial and async-clock to LCC output delay.
- ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
- Test loads are specified in Section 6 of this Data Book.
- "Async. clock" refers to the clock from the Sum term (OR gate).
- The "LCC" term indicates that the timing parameter is applied to the LCC register. The "IOC" term indicates that the timing parameter is applied to the IOC register. The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and IOC registers. The "LCC/IOC/INC" term indicates that the timing parameter is applied to the LCC, IOC and INC registers.
- This refers to the Sum-D gate routed to the IOC register for an additional buried register.
- The term "Input" without any reference to another term refers to an (external) input pin.
- PA7128-1 is an alternate number for PA7128-15.
- PA7128-2 is an alternate number for PA7128-20.
- The parameter t_{SP} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of $(t_{SK} - t_{PK} - t_{IA})$. This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HP} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
- Typical (typ) lcc is measured at $T_A = 25^\circ C$, Freq = 25MHz, $V_{CC} = 5V$.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PA7128P-15	9/15ns	C	P28
PA7128J-15	9/15ns	C	J28
PA7128S-15	9/15ns	C	S28
PA7128P-20	12/20ns	C	P28
PA7128PI-20	12/20ns	I	P28
PA7128J-20	12/20ns	C	J28
PA7128JI-20	12/20ns	I	J28
PA7128S-20	12/20ns	C	S28
PA7128SI-20	12/20ns	I	S28

Part Number

Device Suffix
PA7128P-15

Package

P = Plastic 300mil DIP
 J = Plastic (J) Leaded Chip Carrier
 S = SOIC

Speed

-15 = 9ns/15ns tpd/tpdx
 -20 = 12ns/20ns tpd/tpdx

Temperature Range

(Blank) = Commercial 0 to +70°C
 I = Industrial -40 to +85°C

PA7140 PEELTM Array Programmable Electrically Erasable Logic Array

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Features

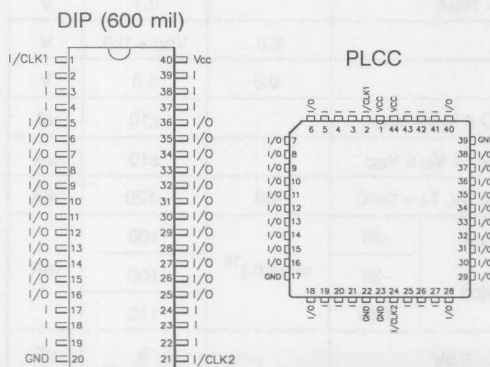
- **CMOS Electrically Erasable Technology**
 - Reprogrammable in 40-pin DIP and 44-pin PLCC packages
- **Versatile Logic Array Architecture**
 - 24 I/Os, 14 inputs, 60 registers/latches
 - Up to 72 logic cell output functions
 - PLA structure with true product-term sharing
 - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
 - Up to 3 output functions per logic cell
 - D, T and JK registers with special features
 - Independent or global clocks, resets, presets, clock polarity, and output enables
 - Sum-of-products logic for output enables
- **High-Speed Commercial and Industrial Versions**
 - As fast as 13ns/20ns (tpdi/tpd), 66.6MHz fmax
 - Industrial grade available for 4.5 to 5.5V Vcc and -40 to +85 °C temperatures
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
 - Integration of multiple PLDs and random logic
 - Buried counters, complex state-machines
 - Comparitors, decoders, other wide-gate functions
- **Development and Programmer Support**
 - ICT PLACE Development Software
 - Fitters for ABEL, CUPL and other software
 - Programming support by ICT PDS-3 and other popular 3rd party programmers

General Description

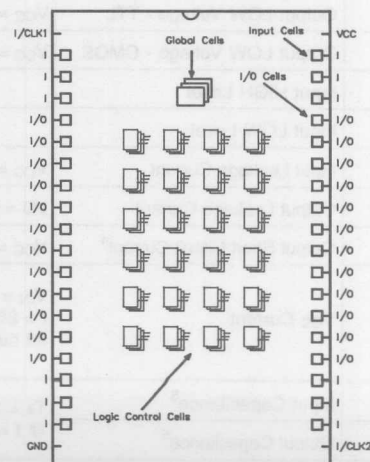
The PA7140 is a member of the Programmable Electrically Erasable Logic (PEEL) Array family based on ICT's 1-micron CMOS EEPROM technology. PEEL Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7140 offers a versatile logic array architecture with 24 I/O pins, 14 input pins and 60 registers/latches (24 buried logic cells, 12 input reg/latches, 24 buried I/O reg/latches). Its logic array implements 100 sum-of-product logic functions divided into two groups each serving 12 logic cells. Each group shares half (60) of the 120 product-terms available for logic cells.

The PA7140's logic and I/O cells (LCCs, IOCs) are extremely flexible with up to three output functions per cell (a total of 72 for all 24 logic cells). Cells are configurable as D, T and JK registers with independent or global clocks, resets, presets, clock polarity, and other features, making the PA7140 suitable for a variety of combinatorial, synchronous, and asynchronous logic applications. The PA7140 supports speeds as fast as 13ns/20ns (tpdi/tpdx) and 66.6MHz (fmax) at moderate power consumption 100mA (80mA typical). Packaging includes 40-pin DIP and 44-pin PLCC. Development and programming support for the PA7140 is provided by ICT and popular third party development tool manufacturers.

Pin Configurations



Block Diagram



This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T _A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T _R	Clock Rise Time	See Note 2		20	ns
T _F	Clock Fall Time	See Note 2		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 2		250	ms

D.C. Electrical Characteristics Over the operating range

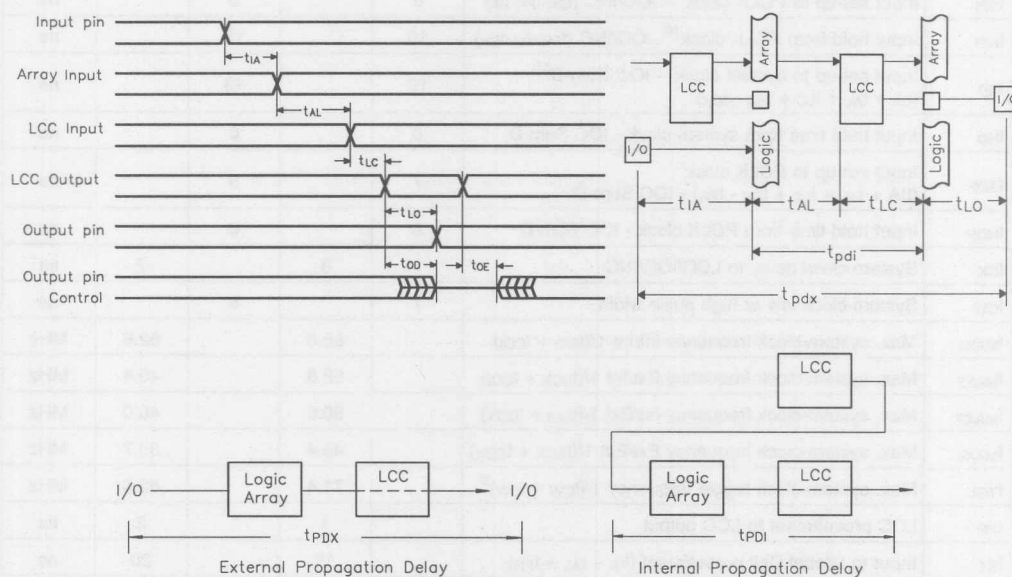
Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage - CMOS	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{OLc}	Output LOW Voltage - CMOS	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		-0.3	0.8	V
I _{IL}	Input Leakage Current	V _{CC} = Max, GND ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V _O ≤ V _{CC}		±10	μA
I _{SC}	Output Short Circuit Current ⁴	V _{CC} = 5V, V _O = 0.5V, T _A = 25°C	-30	-120	mA
I _{CC}	V _{CC} Current	V _{IN} = 0V or V _{CC} ^{3,11} f = 25MHz All outputs disabled	-20	100	mA
			-25	100	
			-1-25	110	
C _{IN}	Input Capacitance ⁵	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT}	Output Capacitance ⁵			12	pF

A.C. Electrical Characteristics Combinatorial

Over the Operating Range

Symbol	Parameter ^{6, 12}	-20 ¹⁷		-25 / I-25 ¹⁷		Unit
		Min	Max	Min	Max	
t _{PDI}	Propagation delay Internal (t _{AL} + t _{LC})		13		17	ns
t _{PDX}	Propagation delay External (t _{IA} + t _{AL} + t _{LC} + t _{LO})		20		25	ns
t _{IA}	Input or I/O pin to array input		2		2	ns
t _{AL}	Array input to LCC		12		16	ns
t _{LC}	LCC input to LCC output ¹⁰		1		1	ns
t _{LO}	LCC output to output pin		5		6	ns
t _{OD} , t _{OE}	Output Disable, Enable from LCC output ⁷		5		6	ns
t _{OX}	Output Disable, Enable from input pin ⁷		20		25	ns

Combinatorial Timing - Waveforms and Block Diagram



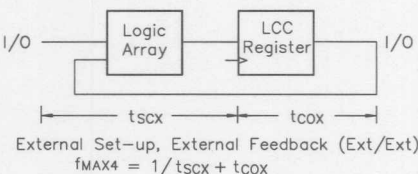
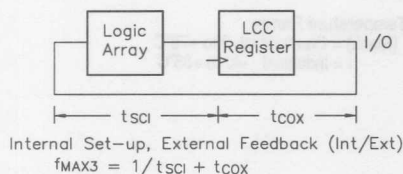
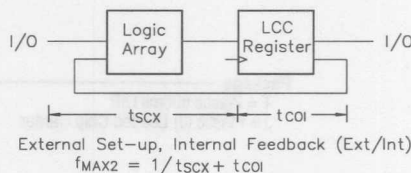
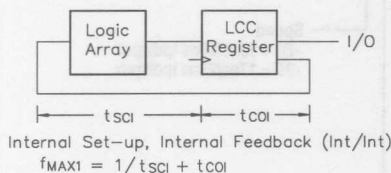
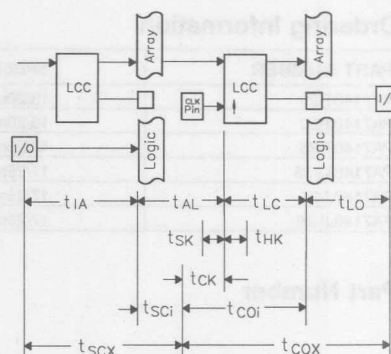
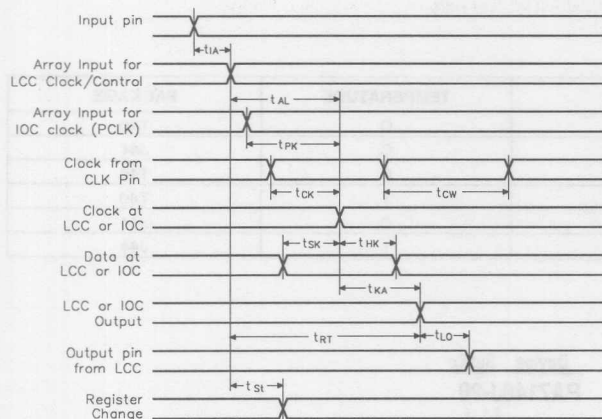
A.C. Electrical Characteristics Sequential

Over the Operating Range

Symbol	Parameter ^{6, 12}	-20 ¹⁷		-25 / I-25 ¹⁷		Unit
		Min	Max	Min	Max	
t _{SCI}	Internal set-up to system-clock ⁸ - LCC ¹⁴ (t _{AL} + t _{SK} + t _{LC} - t _{CK})	8		11		ns
t _{SCX}	Input ¹⁶ (Ext.) set-up to system clock, -LCC (t _{IA} + t _{SCI})	10		14		ns
t _{COI}	System-clock to Array Int. -LCC/IOC/INC ¹⁴ (t _{CK} + t _{LC})		7		8	ns
t _{COX}	System-clock to Output Ext. - LCC (t _{COI} + t _{LO})		12		14	ns
t _{HX}	Input hold time from system clock - LCC	0		0		ns
t _{SK}	LCC input set-up to async. clock ¹³ - LCC	1		1		ns
t _{AK}	Clock at LCC or IOC - LCC output	1		1		ns
t _{HK}	LCC input hold time from async. clock - LCC	4		4		ns
t _{SI}	Input set-up to system clock - IOC/INC ¹⁴ (t _{SK} - t _{CK})	0		0		ns
t _{HI}	Input hold time from system clock - IOC/INC (t _{CK} - t _{SK})	5		6		ns
t _{PK}	Array input to IOC PCLK clock		9		11	ns
t _{SPI}	Input set-up to PCLK clock ¹⁸ - IOC/INC (t _{SK} -t _{PK} -t _{IA})	0		0		ns
t _{HPI}	Input hold from PCLK clock ¹⁸ -IOC/INC (t _{PK} +t _{IA} -t _{SK})	10		12		ns
t _{SD}	Input set-up to system clock - IOC Sum-D ¹⁵ (t _{IA} + t _{AL} + t _{LC} + t _{SK} - t _{CK})	10		13		ns
t _{HD}	Input hold time from system clock - IOC Sum-D	0		0		ns
t _{SDP}	Input set-up to PCLK clock (t _{IA} + t _{AL} + t _{LC} + t _{SK} - t _{PK}) - IOC Sum-D	7		9		ns
t _{HDP}	Input hold time from PCLK clock - IOC Sum-D	0		0		ns
t _{CK}	System-clock delay to LCC/IOC/INC		6		7	ns
t _{CW}	System-clock low or high pulse width	7		8		ns
f _{MAX1}	Max. system-clock frequency Int/Int 1/(t _{SCI} + t _{COI})		66.6		52.6	MHz
f _{MAX2}	Max. system-clock frequency Ext/Int 1/(t _{SCX} + t _{COI})		58.8		45.4	MHz
f _{MAX3}	Max. system-clock frequency Int/Ext 1/(t _{SCI} + t _{COX})		50.0		40.0	MHz
f _{MAX4}	Max. system-clock frequency Ext/Ext 1/(t _{SCX} + t _{COX})		45.4		35.7	MHz
f _{TGL}	Max. system-clock toggle frequency 1/(t _{CW} + t _{CW}) ⁹		71.4		62.5	MHz
t _{PR}	LCC preset/reset to LCC output		1		2	ns
t _{ST}	Input to Global Cell preset/reset (t _{IA} + t _{AL} + t _{PR})		15		20	ns
t _{AW}	Asynch. preset/reset pulse width	8		8		ns
t _{RT}	Input to LCC Reg-Type (RT)		8		10	ns
t _{RTV}	LCC Reg-Type to LCC output register change		1		2	ns
t _{RTC}	Input to Global Cell register-type change (t _{RT} + t _{RTV})		9		12	ns
t _{RW}	Asynch. Reg-Type pulse width	10		10		ns
t _{RESET}	Power-on reset time for registers in clear state ²		5		5	μs

Sequential Timing - Waveforms and Block Diagram

2



Notes:

- Minimum DC input is -0.5V, however inputs may under-shoot to -2.0V for periods less than 20ns.
- Test points for Clock and VCC in t_R , t_F , t_{CL} , t_{CH} , and t_{RESET} are referenced at 10% and 90% levels.
- I/O pins are 0V or VCC.
- Test one output at a time for a duration of less than 1 sec.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$ (See test loads at end of Section 6 for VREF value). t_{OP} is measured from input transition to $VOH - 0.1V$ or $VOL + 0.1V$.
- DIP: "System-clock" refers to pin 1/21 high speed clocks. PLCC: "System-clock" refers to pin 2/24 high speed clocks.
- For T or JK registers in toggle (divide by 2) operation only.
- For combinatorial and async-clock to LCC output delay.
- ICC for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
- Test loads are specified in Section 6 of this Data Book.
- "Async. clock" refers to the clock from the Sum term (OR gate).
- The "LCC" term indicates that the timing parameter is applied to the LCC register. The "IOC" term indicates that the timing parameter is applied to the IOC register. The "LCC/IOC" term indicates that the timing parameter is applied to both the LCC and IOC registers. The "LCC/IOC/INC" term indicates that the timing parameter is applied to the LCC, IOC and INC registers.
- This refers to the Sum-D gate routed to the IOC register for an additional buried register.
- The term "Input" without any reference to another term refers to an (external) input pin.
- PA7140-1 is an alternate number for PA7140-20. PA7140-2 is an alternate number for PA7140-25.
- The parameter t_{SP1} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of $(t_{SK} - t_{PK} - t_{IA})$. This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HP1} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
- Typical (typ) ICC is measured at $T_A = 25^\circ C$, Freq = 25MHz, $V_{CC} = 5V$.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PA7140T-20	13/20ns	C	T40
PA7140J-20	13/20ns	C	J44
PA7140T-25	17/25ns	C	T40
PA7140TI-25	17/25ns	I	T40
PA7140J-25	17/25ns	C	J44
PA7140JI-25	17/25ns	I	J44

Part Number

Device Suffix
PA7140J-20

Package

T = Plastic 600mil DIP
 J = Plastic (J) Leaded Chip Carrier

Speed

-20 = 13ns/20ns tpd/tpdx
 -25 = 17ns/25ns tpd/tpdx

Temperature Range

(Blank) = Commercial 0 to +70°C
 I = Industrial -40 to +85°C

PEEL Devices

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PEEL22CV8 -5, -7, -10, -15, -25	3-35
PEEL20CG10A -5, -7, -10, -15, L-15, -25	3-43
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Introduction to PEEL™ Devices

Simple PLDs

Over the last few years a great deal of attention has been focused on higher pin count Complex PLDs (CPLDs). When first introduced, these newer and larger PLDs were predicted to totally replace Simple PLDs (SPLDs) such as PAL, GAL and PEEL Devices. While CPLDs have their merits, they have not eliminated the demand for SPLDs.

Why the continued popularity of SPLDs? As PACE Technologies PLD Market Analyst, Ronnie Rohleder stated in her Electronic Buyers News column, **"..they're fast, cheap and ease-to-use .. no sophisticated development system is required, and there's a wide range of architectures..."**. The most flexible architectures among SPLDs are provided by PEEL Devices from ICT Inc. See Figure 1.

PEEL Products from ICT Inc.

PEEL Devices are PAL, GAL and EPLD replacements, many of which offer enhanced architectures allowing more logic to be packed into every part. They're ideal for designers who have pushed ordinary PAL/GAL architectures to the limits and need more capability without the cost, complexity and learning curve associated with most CPLDs. PEEL Devices are offered in a wide range of speed and power options.

Development support for PEEL Devices is provided by ICT and popular third party development tool and programmer manufacturers, such as Data I/O. ICT offers the powerful and easy-to-use PLACE Development Software (free to qualified PLD Designers) complete with architectural editor, logic compiler and waveform simulator.

PEEL Device Types

There are two basic types of PEEL Devices: direct replacements and superset replacements. See Table 1.

Direct replacement PEEL Devices include the PEEL 16V8, 20V8, 22CV10A and 22CV10AZ. These devices are JEDEC file and function compatible with

industry-standard architectures. **Superset replacement** PEEL Devices include the PEEL 18CV8, 22CV8, 20CG10A, 22CV10A+ and 22CV10AZ+. These devices provide additional architecture features, beyond those of ordinary SPLDs, such as the 12-configuration macrocell.

Architectural Enhancements

Designing with PEEL Devices is much like designing with other 20 or 24-pin SPLDs. However, superset PEEL Devices give designers greater flexibility with additional inputs, product terms and macrocell configurations. An example of this is shown in Table 2 which compares a standard 16V8/20V8 architecture with an 18CV8/22CV8 enhanced architecture. The following information describes some of the design benefits of PEEL Device enhanced architectures.

Independent Output Enables

Each I/O has independent programmable output enables for both combinatorial or registered outputs. The output enables are helpful for bus interfacing as well as "wire-ORing" of signals. Each I/O can be enabled or disabled via individual product terms, even on registered outputs where most standard PLDs offer only a single output enable control pin.

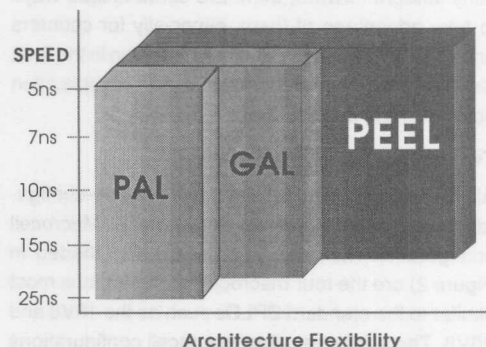


Figure 1. PEEL Devices offer flexible architectures at attractive speeds and prices.

	Architecture						Speed	Power		Key Features
	Pins	Inputs	I/Os	Registers	Macro Config	Product Terms	Tpd (ns) (min)	Icc(mA) (Typ)	Icc (mA) (max)	
Direct Replacement										
PEEL16V8	20	8	8	8	4	64	25, 15 10, 7, 5	45 - 75	55 - 115	Pin and JEDEC file compatible with PAL/GAL 16V8s and 20V8s
PEEL20V8	24	12								
PEEL22CV10A	24	12	10	10	4	132	25, 15 10, 7, 5	40 - 100	67 - 155	Pin and JEDEC file compatible with standard 22V10s, Low and Zero power versions
PEEL22CV10AZ								25µA (3.5@ 1MHz)	100µA (5.0@ 1MHz)	
Superset Replacement										
PEEL18CV8	20	10	8	8	12	74	25, 15 10, 7, 5	18 - 75	37 - 110	Pin-compatible superset of 20/24-pin PAL/GAL/ EPLD, lower power
PEEL22CV8	24	14						10 - 75	15 - 90	
PEEL20CG10A	24	12	10	10	12	92	25, 15 10, 7, 5	40 - 100	67 - 155	Pin compatible superset of 24-pin PAL/GAL/EPLD
PEEL22CV10A+*	24	12	10	10	12	132	25, 15 10, 7, 5	40 - 100	67 - 155	Pin compatible superset of standard 22V10s, 12-config. macrocell
PEEL22CV10AZ+*								25µA (3.5@ 1MHz)	100µA (5.0@ 1MHz)	Zero power version also has P-term clock and clock polarity

* The "+" indicates the "plus" mode, a software/programming option that allows the standard 22CV10A and 22V10AZ to use extra architecture features.

Table 1. PEEL Devices Selection Guide

Global Preset and Clear

The PEEL18CV8, 22CV8, 20CG10A, 22CV10A and 22CV10AZ each have a synchronous preset (SP) and asynchronous clear (AC) product term that control all the registers. Although these functions are fairly straight forward, there are some unique ways to take advantage of them, especially for counters and state machines. An example is shown in the 8-bit Counter with Function Controls design in application note AN-1A in this data book.

Twelve-Configuration Macrocell

All of ICT's superset SPLDs have a twelve-configuration macrocell as shown in Figure 2. Macrocell configuration numbers 3, 4, 9 and 10 (shaded in Figure 2) are the four macrocell configurations most similar to the standard SPLDs such as the 16V8 and 20V8. The additional eight macrocell configurations (1, 2, 5, 6, 7, 8, 11, and 12) can be used for a variety

Architecture Features	16V8/ 20V8	18CV8/ 22CV8
Pin Count	20/24	20/24
Inputs (into array)	16/20	18/22
Outputs	8	8
Feedbacks	6 or 8 *	8
Product Terms	64	74
Reg. Output Enables	shared pin	p-terms
Preset/Clear P-terms	no	yes
Clock avail. to array	no	yes
Macro. Configurations	4	12
Buried Combinatorial	no	yes
Buried Registers	no	yes **
Design Modes	3 modes: Simple Complex Registered	no modes needed, all macrocell configurations available

* Depends on Design Mode ** Pseudo- Buried Register

Table 2. SPLD Architecture Comparisons

of logic functions not possible with ordinary SPLDs. These functions include:

- Bi-Directional Registered I/O
- Buried Combinatorial Feedback
- Buried Combinatorial Feedback with Register
- Buried Register with Combinatorial Output

The flexible output enable and register preset/clear controls can be used together with the extra macro-cell configurations to implement a wide range of designs that won't fit into other devices. See AN-1A for design tricks and techniques that show details of how to use the enhanced PEEL Device architecture for real applications.

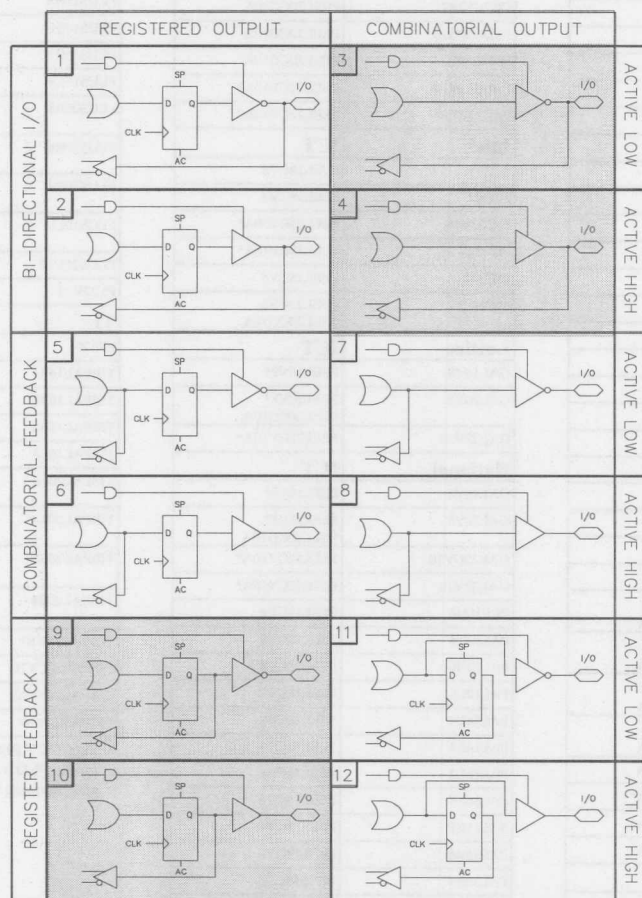
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Figure 2. PEEL Device 12-Configuration Macrocell.



Quick PEEL Device Cross Reference

V2.0

Altera	ICT
EP310	PEEL18CV8
EP320	PEEL18CV8
EP330	PEEL18CV8
AMD	ICT
AmPAL18P8	PEEL18CV8
AmPAL20L10	PEEL20CG10A
AmPAL22P10	PEEL20CG10A
AmPAL22V10	PEEL22CV10A*
PAL10H8	PEEL18CV8
PAL10L8	PEEL18CV8
PAL12H6	PEEL18CV8
PAL12L6	PEEL18CV8
PAL14H4	PEEL18CV8
PAL14L4	PEEL18CV8
PAL16H2	PEEL18CV8
PAL16HD8	PEEL18CV8
PAL16L2	PEEL18CV8
PAL16RP4	PEEL18CV8
PAL16RP6	PEEL18CV8
PAL16RP8	PEEL18CV8
PALC16L8	PEEL18CV8
PALC16R4	PEEL18CV8
PALC16R6	PEEL18CV8
PALC16R8	PEEL18CV8
PALC18U8	PEEL18CV8
PALCE16V8	PEEL16V8*
PALC16R8	PEEL18CV8
PALC18U8	PEEL18CV8
PAL16L8	PEEL18CV8
PAL16R4	PEEL18CV8
PAL16R6	PEEL18CV8
PAL16R8	PEEL18CV8
PAL20R4	PEEL22CV8 PEEL20CG10A
PAL20R6	PEEL22CV8 PEEL20CG10A
PAL20R8	PEEL22CV8 PEEL20CG10A
PALCE20V8	PEEL20V8* PEEL20CG10A
PAL20L10	PEEL20CG10A
PAL22V10	PEEL22CV10A*
AMPAL22V10	PEEL22CV10A*
PALCE22V10	PEEL22CV10A*
AMI	ICT
PEEL18CV8	PEEL18CV8*
PEEL20CG10	PEEL20CG10A*
PEEL22CV10	PEEL22CV10A*
Atmel	ICT
ATF16V8	PEEL16V8*
ATF20V	PEEL20V8*
ATF22V10	PEEL22CV10A*

Cypress	ICT
PALC16R8	PEEL18CV8
PALC16R6	PEEL18CV8
PALC16R4	PEEL18CV8
PAL16R4	PEEL18CV8
PAL16L8	PEEL18CV8
PAL16R8	PEEL18CV8
PAL16R6	PEEL18CV8
PAL16R4	PEEL18CV8
PLDC18G8	PEEL18CV8
PLDC20G10	PEEL20CG10A
CG7C323B	PEEL20CG10A
PLDC20G10	PEEL20CG10A
PLD20G10	PEEL20CG10A
PALC22V10	PEEL22CV10A*
PAL22VP10	PEEL22CV10A*
Intel	ICT
5CO31	PEEL18CV8
5CO32	PEEL18CV8
85C22V10	PEEL22CV10A*
PLD22V10	PEEL22CV10A*
85C220	PEEL18CV8
85C224	PEEL22CV8 PEEL20CG10A
Lattice	ICT
GAL16V8	PEEL16V8*
GAL20V8	PEEL20V8* PEEL20CG10A
GAL22V10	PEEL22CV10A*
National	ICT
GAL16V8	PEEL16V8*
GAL20V8	PEEL20V8* PEEL20CG10A
GAL22CV10	PEEL22CV10A*
GAL22V10	PEEL22CV10A*
PAL10H8	PEEL18CV8
PAL10L8	PEEL18CV8
PAL12H6	PEEL18CV8
PAL12L6	PEEL18CV8
PAL14H4	PEEL18CV8
PAL14L4	PEEL18CV8
PAL16L2	PEEL18CV8
PAL16L8	PEEL18CV8
PAL16R8	PEEL18CV8
PAL16R6	PEEL18CV8
PAL16R4	PEEL18CV8
PAL12L10	PEEL20CG10A
PAL14L8	PEEL22CV8
PAL16L6	PEEL22CV8
PAL18L4	PEEL22CV8
PAL20L2	PEEL22CV8
PAL20L8	PEEL22CV8
PAL20L10	PEEL20CG10A

PAL20P8	PEEL20CG10A
PAL20R8	PEEL22CV8 PEEL20CG10A
PAL20R6	PEEL22CV8 PEEL20CG10A
PAL20R4	PEEL22CV8 PEEL20CG10A
PAL20RP8	PEEL22CV8 PEEL20CG10A
PAL10RP6	PEEL22CV8 PEEL20CG10A
PAL20RP4	PEEL22CV8 PEEL20CG10A
Philips	ICT
PLUS16R8	PEEL18CV8
PLUS16R6	PEEL18CV8
PLUS16R4	PEEL18CV8
PLUS16L8	PEEL18CV8
PLUS20R8	PEEL22CV8 PEEL20CG10A
PLUS20R6	PEEL22CV8 PEEL20CG10A
PLUS20R4	PEEL22CV8 PEEL20CG10A
PLUS20L8	PEEL22CV8 PEEL20CG10A
PLUS22V10	PEEL22CV10A*
PL22V10	PEEL22CV10A*
TI	ICT
EP330	PEEL18CV8
TIBPAL16R4	PEEL18CV8
TIBPAL16R6	PEEL18CV8
TIBPAL16R8	PEEL18CV8
TIBPAL16L8	PEEL18CV8
TIBPAL20L8	PEEL22CV8 PEEL20CG10A
TIBPAL20R4	PEEL22CV8 PEEL20CG10A
TIBPAL20R6	PEEL22CV8 PEEL20CG10A
TIBPAL20R8	PEEL22CV8 PEEL20CG10A
TIBPAL22V10	PEEL22CV10A*
TIBPAL22CV10	PEEL22CV10A*
TIBPAL22VP10	PEEL22CV10A*
TICPAL22V10	PEEL22CV10A*

* These ICT PEEL devices are plug-in replacements for the PLD's listed using the existing Jeduc programming file.

PEEL™ 16V8 -5/-7/-10/-15/-25 CMOS Programmable Electrically Erasable Logic

Features

- **Compatible with Popular 16V8 Devices**
 - 16V8 socket and function compatible
 - Programs with standard 16V8 JEDEC file
 - 20-pin DIP, SOIC, and PLCC packages
- **CMOS Electrically Erasable Technology**
 - Superior factory testing
 - Reprogrammable in plastic package
 - Reduces retrofit and development costs
- **Application Versatility**
 - Replaces random logic
 - Super-sets standard 20-pin PLDs (PALs)
- **Low Power and Quarter Power Versions**
 - Low Power: 75mA typical I_{CC}
 - Quarter Power: 45mA typical I_{CC}
- **Development/Programmer Support**
 - Third party software and programmers
 - ICT PLACE Development Software and PDS-3 programmer
 - Automatic programmer translation and JEDEC file translation software available for the most popular PAL devices

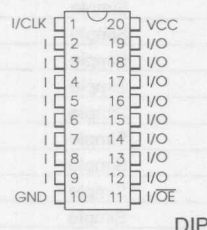
3

General Description

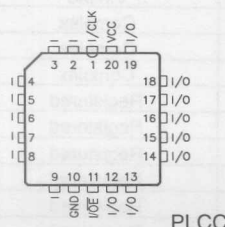
The PEEL16V8 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL16V8 offers the performance, flexibility, ease-of-design, and production practicality needed by logic designers today. The PEEL16V8 is available in 20-pin DIP, PLCC and SOIC packages (see Figure 1) with speeds ranging from 5ns to 25ns and power consumption as low as 45mA. EE-reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-reprogrammability also improves fac-

tory testability, thus ensuring the highest quality possible. The PEEL16V8 architecture allows it to replace standard 20-pin PAL devices. See Figure 2. ICT's PEEL16V8 can be programmed with any existing 16V8 JEDEC file. Some programmers also allow the PEEL16V8 to be programmed directly from PAL 16L8, 16R4, 16R6 and 16R8 JEDEC files. Additional development and programming support for the PEEL16V8 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

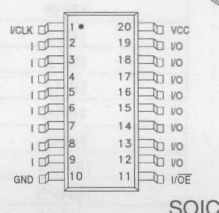
Pin Configuration (Figure 1)



DIP

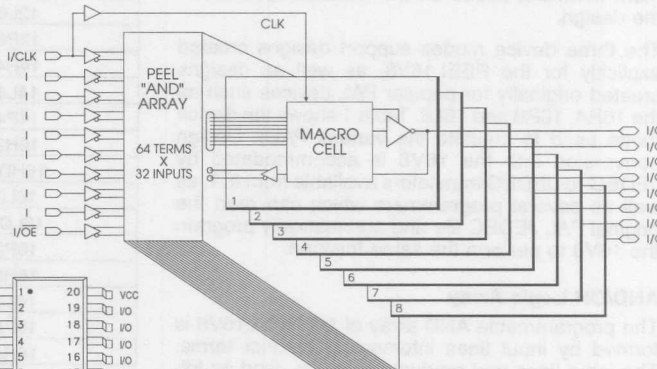


PLCC



SOIC

Block Diagram (Figure 2)



Functional Description

The PEEL16V8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of macrocells further increase logic flexibility.

Architecture Overview

The PEEL16V8 features ten dedicated input pins and eight I/O pins, which allow a total of up to 16 inputs and 8 outputs for creating logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL16V8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the eight OR functions is a macrocell which can be independently programmed to one of up to four different basic configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing two possible feedback paths into the array.

Three different device modes, Simple, Complex, and Registered, support various user configurations. In Simple mode a macrocell can be configured for combinatorial function with the output buffer permanently enabled, or the output buffer can be disabled and the I/O pin used as a dedicated input. In Complex mode a macrocell is configured for combinatorial function with the output buffer enable controlled by a product term. In Registered mode, a macrocell can be configured for registered operation with the register clock and output buffer enable controlled directly from pins, or can be configured for combinatorial function with the output buffer enable controlled by a product term. In most cases the device mode is set automatically by the development software, based on the features specified in the design.

The three device modes support designs created explicitly for the PEEL16V8, as well as designs created originally for popular PAL devices such as the 16R4, 16R8 and 16L8. Table 1 shows the device mode used to emulate the various PALs. Design conversion into the 16V8 is accommodated by JEDEC-to-JEDEC translators available from ICT, as well as several programmers which can read the original PAL JEDEC file and automatically program the 16V8 to perform the same function.

AND/OR Logic Array

The programmable AND array of the PEEL16V8 is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

32 input lines:

16 input lines carry the true and complement of the signals applied to the 8 dedicated input pins

16 additional lines carry the true and complement of 8 macrocell feedback signals or inputs from I/O pins or the clock/OE pins

64 product terms:

56 product terms (arranged in 8 groups of 7) form sum-of-product functions for macrocell combinatorial or registered logic

8 product terms (arranged 1 per macrocell) add an additional product term for macrocell sum-of-products functions or I/O pin output enable control

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 32-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, that term will always be TRUE.

When programming the PEEL16V8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function.)

Table 1. PEEL16V8/PAL Device Compatibility

PAL Architecture Compatibility	PEEL16V8 Device Mode
10H8	Simple
10L8	Simple
10P8	Simple
12H6	Simple
12L6	Simple
12P6	Simple
14H4	Simple
14L4	Simple
14P4	Simple
16H2	Simple
16HD8	Simple
16L2	Simple
16LD8	Simple
16P2	Simple
16H8	Complex
16L8	Complex
16P8	Complex
16R4	Registered
16R6	Registered
16R8	Registered
16RP4	Registered
16RP6	Registered
14RP8	Registered

Programmable Macrocell

The macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL16V8 to the precise requirements of their designs.

Macrocell Architecture

Each macrocell consists of an OR function, a D-type flip-flop, an output polarity selector, and a programmable feedback path. Four EEPROM architecture bits MS0, MS1, OP and RC control the configuration of each macrocell. Bits MS0 and MS1 are global, and select between Simple, Complex and Registered mode for the whole device. Bits OP and RC are local for each macrocell; bit OP controls the output polarity and bit RC selects between registered and combinatorial operation and also specifies the feedback path. Table 2 shows the architecture bit settings for each possible configuration.

Equivalent circuits for the possible macrocell configurations are illustrated in Figures 3, 4 and 5. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Simple Mode

In Simple mode, all eight product terms feed the OR array which can generate a purely combinatorial function for the output pin. The programmable output polarity selector allows active-high or active-low logic, eliminating the need for external inverters. For output functions, the buffer can be permanently enabled. Feedback into the array is available on all

macrocell I/O pins, except for pins 15 and 16. Figure 6 shows the logic array of the PEEL16V8 configured in Simple mode.

Simple mode also provides the option of configuring an I/O pin as a dedicated input. In this case the output buffer is permanently disabled, and the I/O pin feedback is used to bring the input signal from the pin into the logic array. This option is available for all I/O pins except pins 15 and 16.

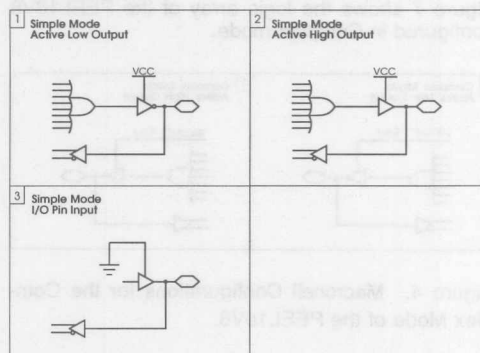


Figure 3. Macrocell Configurations for the Simple Mode of the PEEL16V8

Table 2. PEEL16V8 Device Mode/Macrocell Configuration Bits

Config. #	Mode	Architecture Bits				Function	Polarity	Feedback
		MS0	MS1	OP	RC			
1	Simple	1	0	0	0	Combinatorial	Active Low	I/O Pin
2	Simple	1	0	1	0	Combinatorial	Active High	I/O Pin
3	Simple	1	0	X	1	None	None	I/O Pin
1	Complex	1	1	0	1	Combinatorial	Active Low	I/O Pin
2	Complex	1	1	1	1	Combinatorial	Active High	I/O Pin
1	Registered	0	1	0	0	Registered	Active Low	Registered
2	Registered	0	1	1	0	Registered	Active High	Registered
3	Registered	0	1	0	1	Combinatorial	Active Low	I/O Pin
4	Registered	0	1	1	1	Combinatorial	Active High	I/O Pin

Complex Mode

In Complex mode, seven product terms feed the OR array which can generate a purely combinational function for the output pin. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. The output buffer is controlled by the eighth product term, allowing the macrocell to be configured for input, output or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all pins except 12 and 19. Figure 7 shows the logic array of the PEEL16V8 configured in Complex mode.

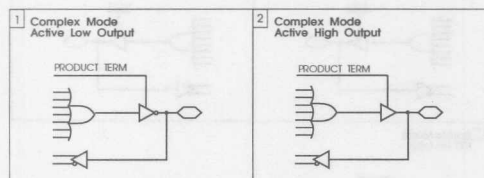


Figure 4. Macrocell Configurations for the Complex Mode of the PEEL16V8

Registered Mode

Registered mode provides eight product terms to the OR array for registered functions. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. (Note, however, that PEEL16V8 registers power-up reset and so before the first clock arrives the output at the pin will be low if the user has selected active-high logic and high if the user has selected active-low logic.) For registered functions, the output buffer enable is controlled directly from the /OE control pin. Feedback into the array comes from the macrocell register. In Registered mode, input pins 1 and 11 are permanently allocated as CLK and /OE, respectively. Figure 8 shows the logic array of the PEEL16V8 configured in Registered mode.

Registered mode also provides the option of configuring a macrocell for combinational operation, with seven product terms feeding the OR function.

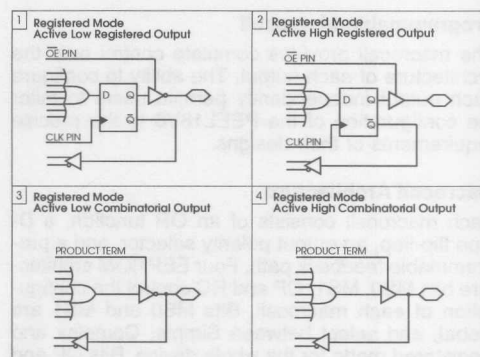


Figure 5. Macrocell Configurations for the Registered Mode of the PEEL16V8

Again the programmable output polarity selector provides active-high or active-low logic. The output buffer enable is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all I/O pins.

Design Security

The PEEL16V8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit has been set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL16V8. The code cannot be read back after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

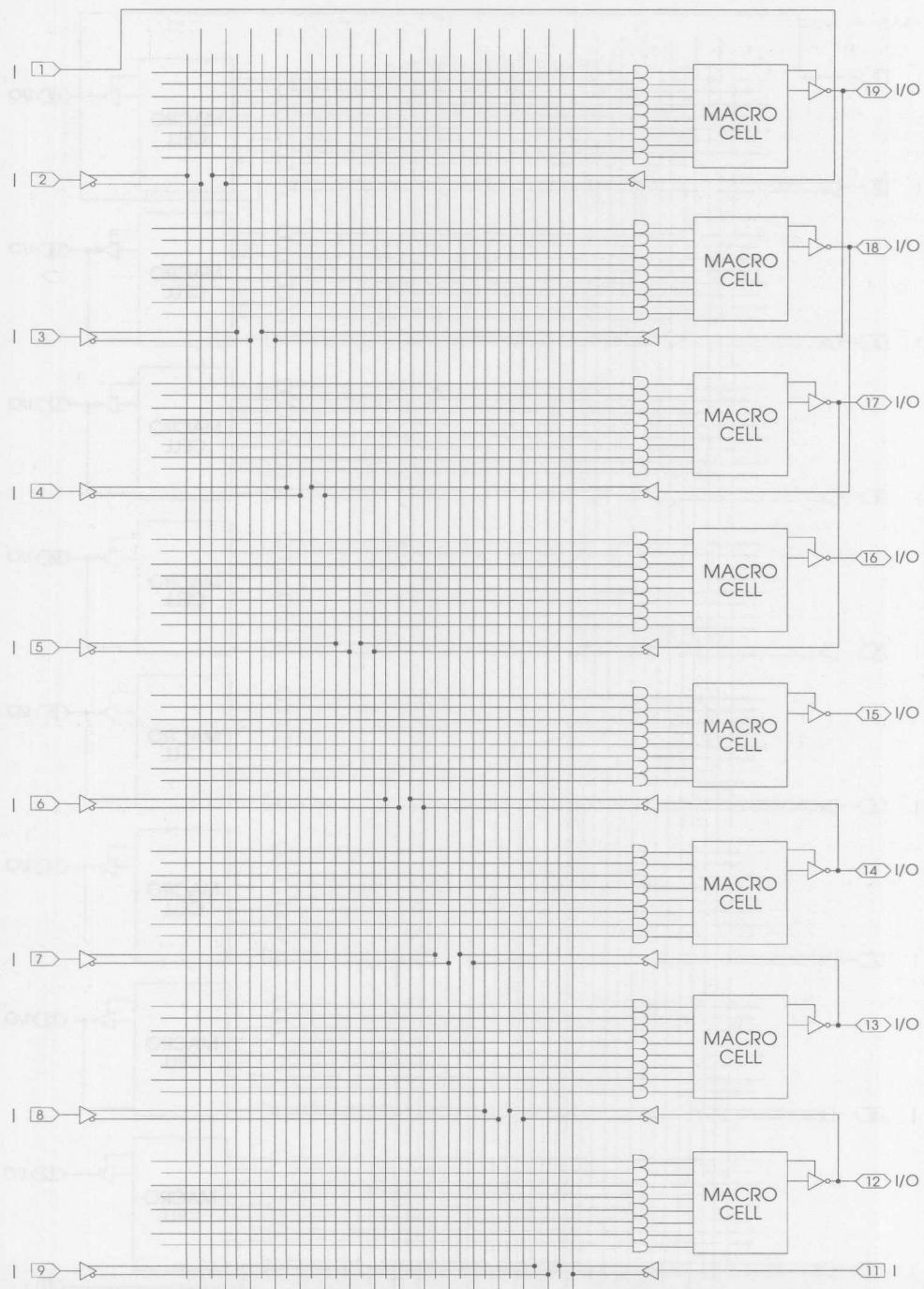


Figure 6. PEEL16V8 Logic Array - Simple Mode

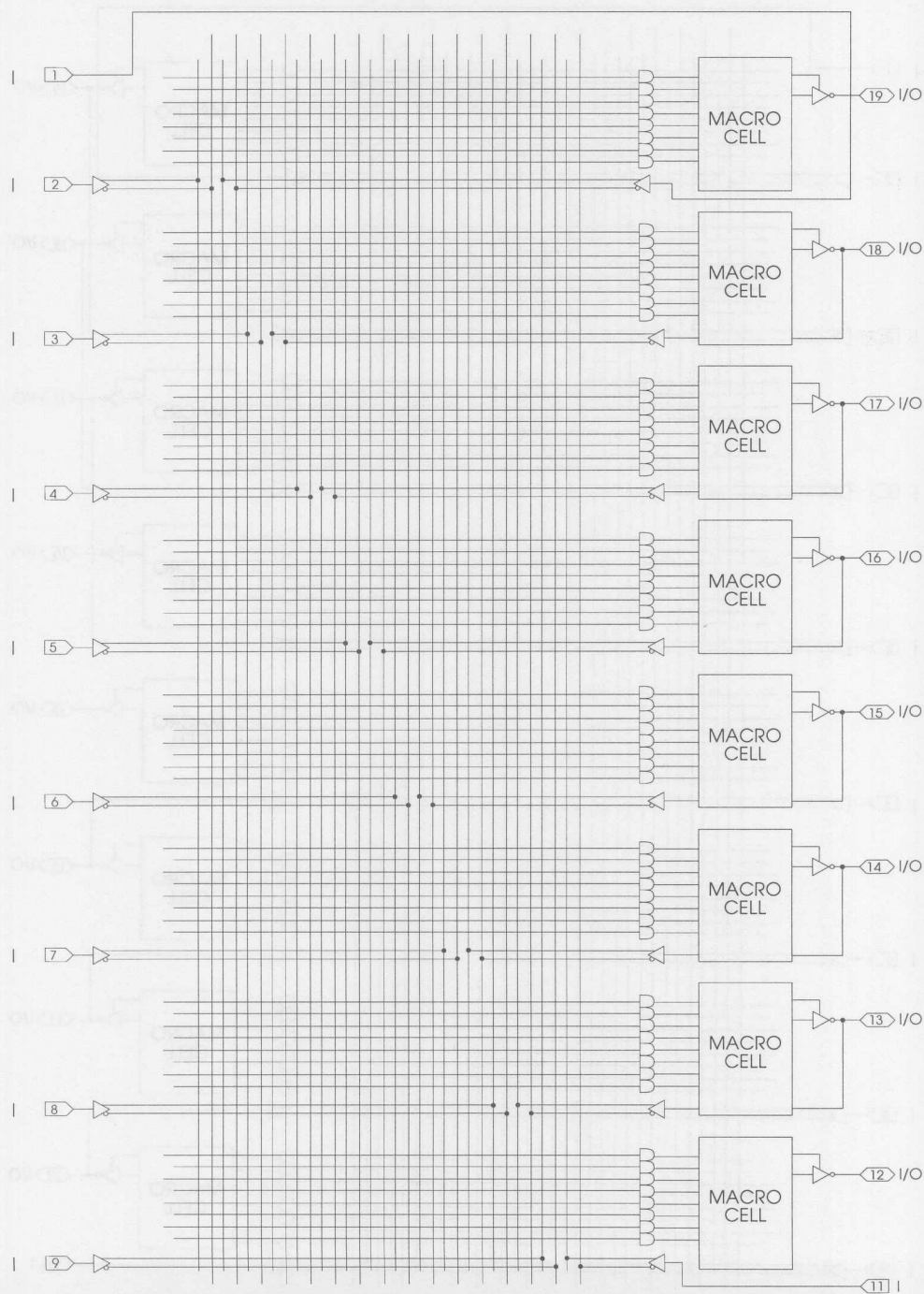


Figure 7. PEEL16V8 Logic Array - Complex Mode

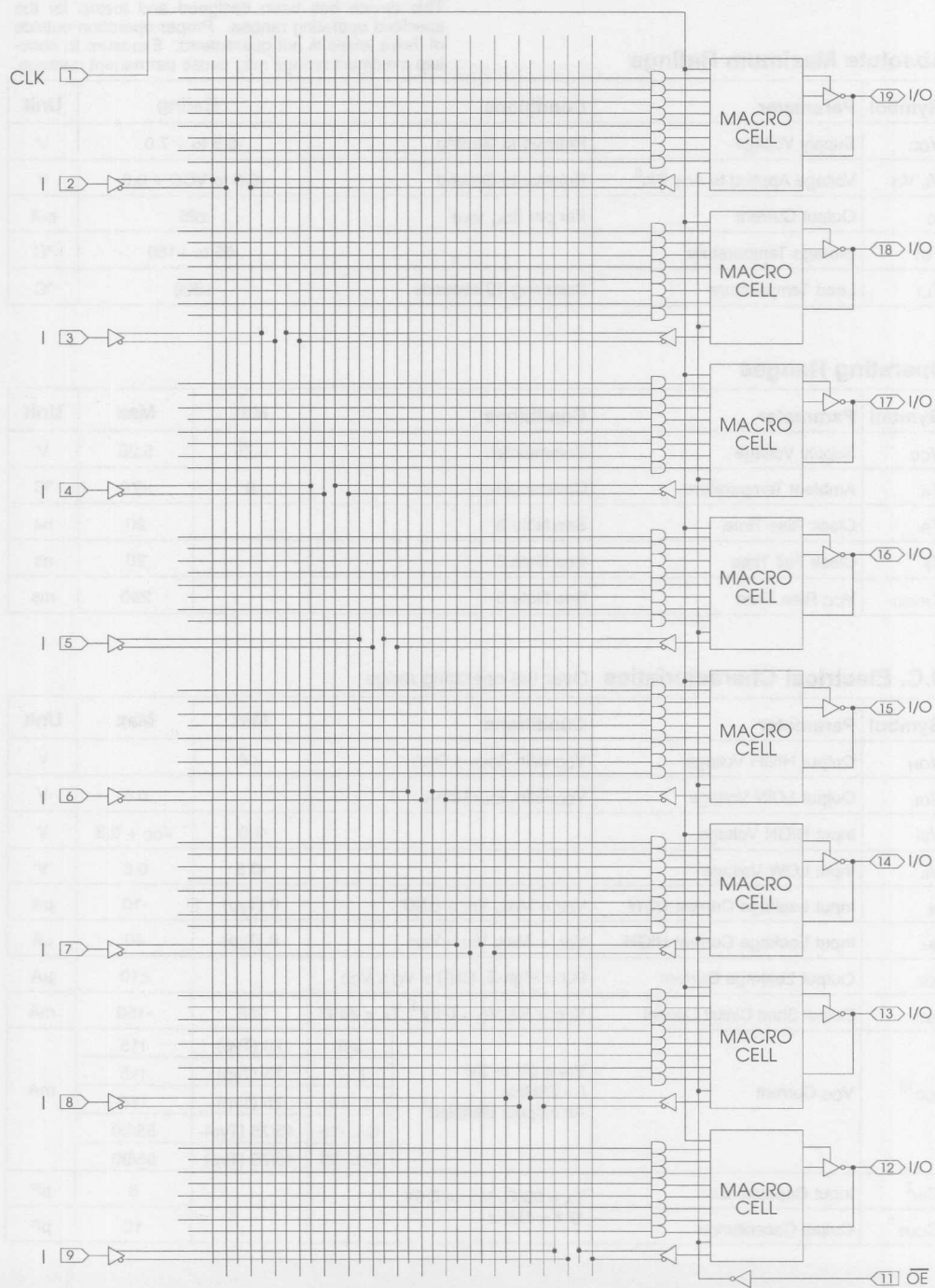


Figure 8. PEEL16V8 Logic Array - Registered Mode

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
T _A	Ambient Temperature	Commercial	0	+70	°C
T _R	Clock Rise Time	See Note 3		20	ns
T _F	Clock Fall Time	See Note 3		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 3		250	ms

D.C. Electrical Characteristics Over the operating range

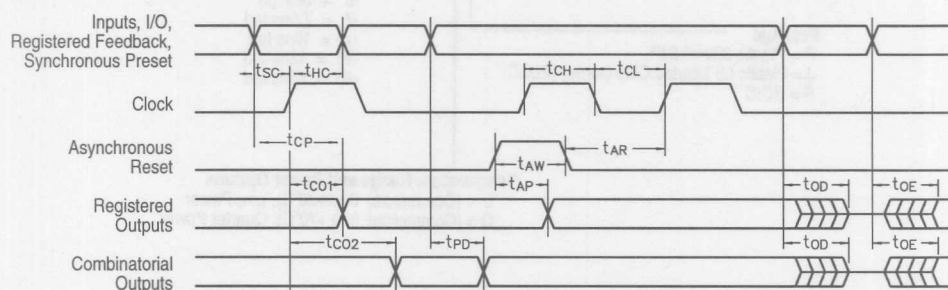
Symbol	Parameter	Conditions		Min	Max	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min, I _{OH} =-4.0mA		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} =Min, I _{OL} =16mA			0.5	V
V _{IH}	Input HIGH Voltage			2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage			-0.3	0.8	V
I _{IL}	Input Leakage Current LOW	V _{CC} = Max, V _{IN} = GND		0 (Typ)	-10	μA
I _{IH}	Input Leakage Current HIGH	V _{CC} = Max, V _{IN} = V _{CC}		0 (Typ)	40	μA
I _{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V _O ≤ V _{CC}			±10	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5V, V _O = 0.5V ⁹ , T _A = 25°C		-30	-150	mA
I _{CC} ¹⁰	V _{CC} Current	V _{IN} = 0V or 3V f = 25MHz All outputs disabled ⁴	L-5	75 (Typ)	115	mA
			L -7	75 (Typ)	115	
			L -10	75 (Typ)	115	
			Q/L -15	45/75 (Typ)	55/90	
			Q/L -25	45/75 (Typ)	55/90	
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz			6	pF
C _{OUT} ⁷	Output Capacitance				12	pF

A.C. Electrical Characteristics

Over the Operating Range ^{8, 11}

Symbol	Parameter	L-5		L-7		L-10		Q/L-15		Q/L-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD}	Input ⁵ to non-registered output	1	5	3	7.5	3	10	3	15	3	25	ns
t _{OE}	Input ⁵ to output enable ⁶	1	6	3	7.5	3	10	3	15	3	20	ns
t _{OD}	Input ⁵ to output disable ⁶	1	5	3	7.5	3	10	3	15	3	20	ns
t _{CO1}	Clock to output	1	4	2	7	2	7	2	10	2	12	ns
t _{CO2}	Clock to comb. output delay via internal registered feedback		7.5		10		12		25		35	ns
t _{CF}	Clock to Feedback		3		3.5		4		8		10	ns
t _{SC}	Input ⁵ or feedback setup to clock	3		5		5		12		15		ns
t _{HC}	Input ⁵ hold after clock	0		0		0		0		0		ns
t _{CL} , t _{CH}	Clock low time, clock high time ⁸	3		3.5		5		8		12		ns
t _{CP}	Min clock period Ext (t _{SC} + t _{CO1})	7		12		12		22		27		ns
f _{MAX1}	Internal Feedback (1/t _{SC} +t _{CF}) ¹²	166.6		117.6		111.1		50		40		MHz
f _{MAX2}	External Feedback (1/t _{CP}) ¹²	142.8		83.3		83.3		45.5		37		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹²	166.6		142.8		100		62.5		41.6		MHz
t _{AW}	Asynchronous Reset pulse width	5		7.5		10		15		25		ns
t _{AP}	Input ⁵ to Asynchronous Reset		5		7.5		10		15		25	ns
t _{AR}	Asynch. Reset recovery time		5		7.5		10		15		25	ns
t _{RESET}	Power-on reset time for registers in clear state		5		5		5		5		5	μs

Switching Waveforms



Notes

- Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
- V_I and V_O are not specified for program/verify operation.
- Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
- I/O pins are 0V and 3V.
- "Input" refers to an Input pin signal.
- t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; V_{REF} = V_L see test loads in Section 6 of this Data Book.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- Test one output at a time for a duration of less than 1 sec.
- ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
- PEEL Device test loads are specified in Section 6 of this Data Book.
- Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL16V8JL-5	5ns	C	J20
PEEL16V8PL-7	7.5ns	C	P20
PEEL16V8JL-7	7.5ns	C	J20
PEEL16V8SL-7	7.5ns	C	S20
PEEL16V8PL-10	10ns	C	P20
PEEL16V8JL-10	10ns	C	J20
PEEL16V8SL-10	10ns	C	S20
PEEL16V8PL-15	15ns	C	P20
PEEL16V8PQ-15	15ns	C	P20
PEEL16V8JL-15	15ns	C	J20
PEEL16V8JQ-15	15ns	C	J20
PEEL16V8SL-15	15ns	C	S20
PEEL16V8SQ-15	15ns	C	S20
PEEL16V8PL-25	25ns	C	P20
PEEL16V8PQ-25	25ns	C	P20
PEEL16V8JL-25	25ns	C	J20
PEEL16V8JQ-25	25ns	C	J20
PEEL16V8SL-25	25ns	C	S20
PEEL16V8SQ-25	25ns	C	S20

Part Number

Device Suffix
PEEL16V8PL-25

Package
 P = Plastic 300mil DIP
 J = Plastic (J) Leaded Chip Carrier (PLCC)
 S = SOIC

Speed
 -5 = 5ns tpd
 -7 = 7.5ns tpd
 -10 = 10ns tpd
 -15 = 15ns tpd
 -25 = 25ns tpd

Temperature Range and Power Options
 L = (Commercial 0 to +70°C), Low Power
 Q = (Commercial 0 to +70°C), Quarter Power

PEEL™ 18CV8 -5/-7/-10/-15/-25 CMOS Programmable Electrically Erasable Logic Device

3

Features

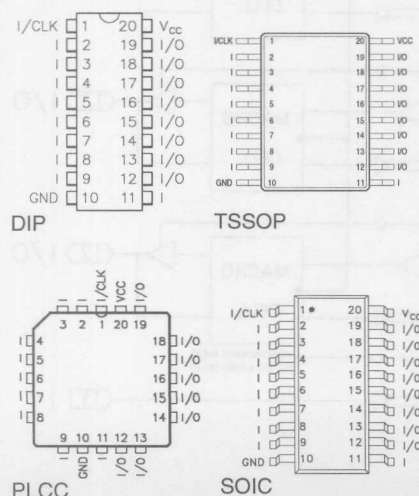
- **Multiple Speed, Power, Temperature Options**
 - Speeds ranging from 5ns to 25ns
 - Power as low as 37mA at 25MHz
 - Commercial and industrial versions available
- **CMOS Electrically Erasable Technology**
 - Superior factory testing
 - Reprogrammable in plastic package
 - Reduces retrofit and development costs
- **Development/Programmer Support**
 - Third party software and programmers
 - ICT PLACE Development Software and PDS-3 programmer
 - PLD-to-PEEL JEDEC file translator
- **Architectural Flexibility**
 - 74 product term x 36 input array
 - Up to 18 inputs and 8 I/O pins
 - 12 possible macrocell configurations
 - Synchronous preset, asynchronous clear
 - Independent Output enables
 - 20-pin DIP, PLCC, SOIC and TSSOP packages
- **Application Versatility**
 - Replaces random logic
 - Super-sets standard PLDs (PAL, GAL, EPLD)
 - Enhanced Architecture fits more logic than ordinary PLDs

General Description

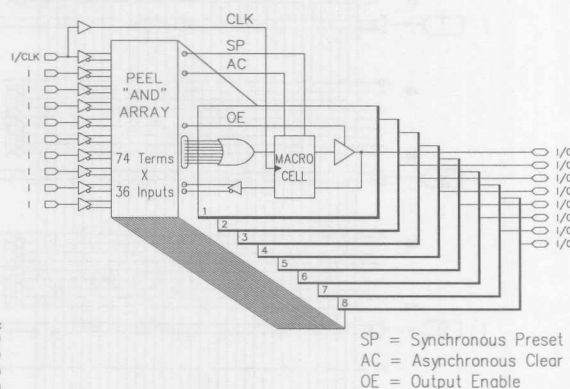
The PEEL18CV8 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL18CV8 offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL18CV8 is available in 20-pin DIP, PLCC, SOIC and TSSOP packages with speeds ranging from 5ns to 25ns with power consumption as low as 37mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves fac-

tory testability, thus assuring the highest quality possible. The PEEL18CV8 architecture allows it to replace over 20 standard 20-pin PLDs (PAL, GAL, EPLD, etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts to the PEEL18CV8 existing 20-pin PLDs without the need to rework the existing design. Development and programming support for the PEEL18CV8 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



Block Diagram (Figure 2)



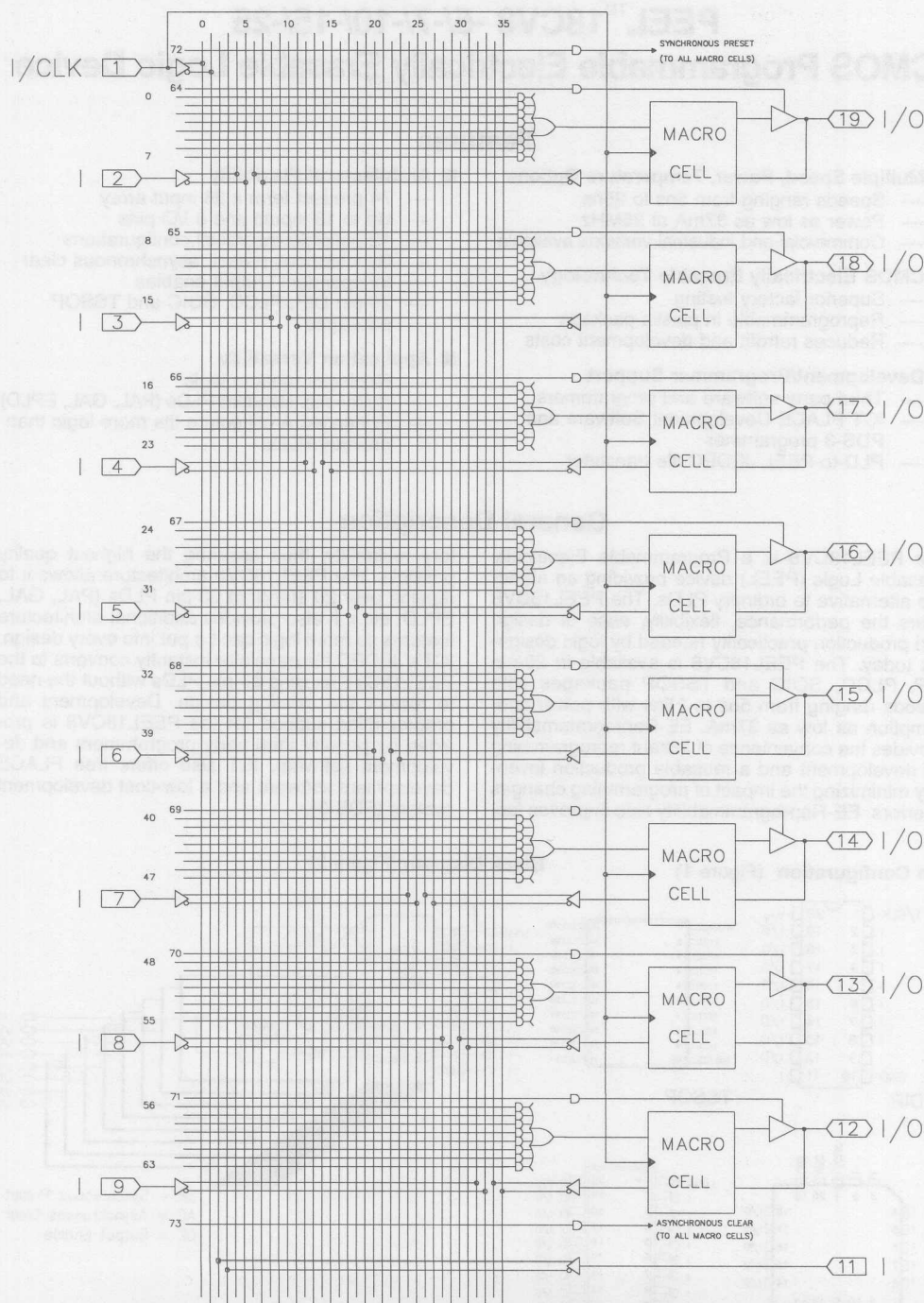


Figure 3. PEEL18CV8 Logic Array Diagram

Function Description

The PEEL18CV8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL18CV8 architecture is illustrated in the block diagram of Figure 2. Ten dedicated inputs and 8 I/Os provide up to 18 inputs and 8 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL18CV8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the 8 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL18CV8 (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

36 Input Lines:

- 20 input lines carry the true and complement of the signals applied to the 10 input pins
- 16 additional lines carry the true and complement values of feedback or input signals from the 8 I/Os

74 product terms:

- 64 product terms (arranged in groups of 8) used to form sum of product functions
- 8 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 36-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE.

When programming the PEEL18CV8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is con-

figured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function).

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL18CV8 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Refer to Table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9 and 10) the macrocell provides eight additional configurations. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL18CV8 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output of the OR gate,

bypassing the output buffer, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7 and 8 in Figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing combinatorial output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Design Security

The PEEL18CV8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

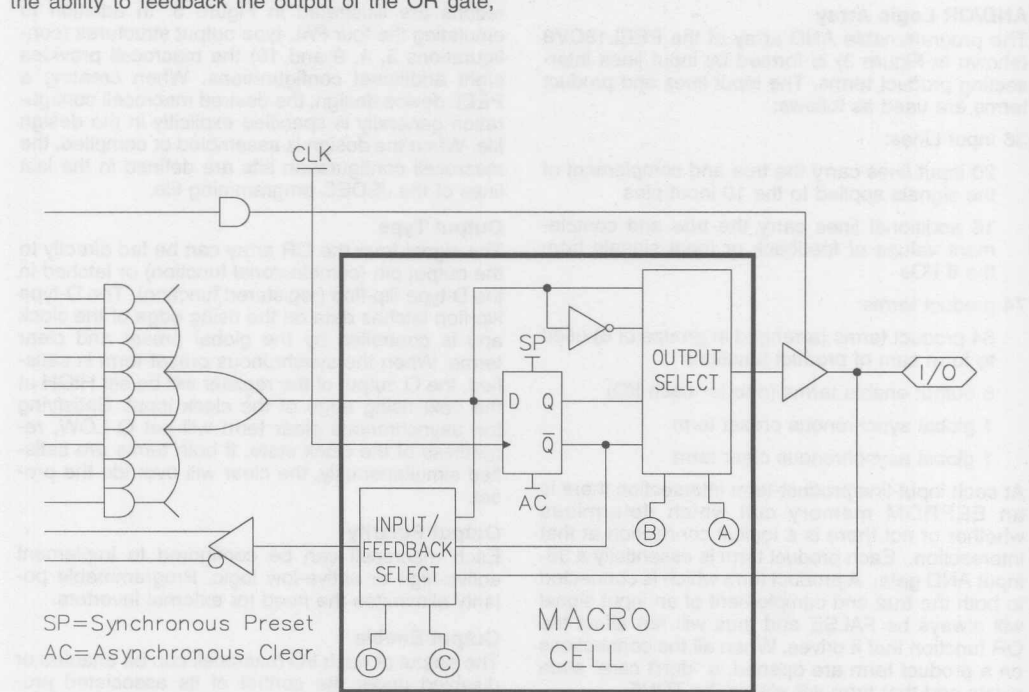


Figure 4. Block Diagram of The PEEL18CV8 I/O Macrocell

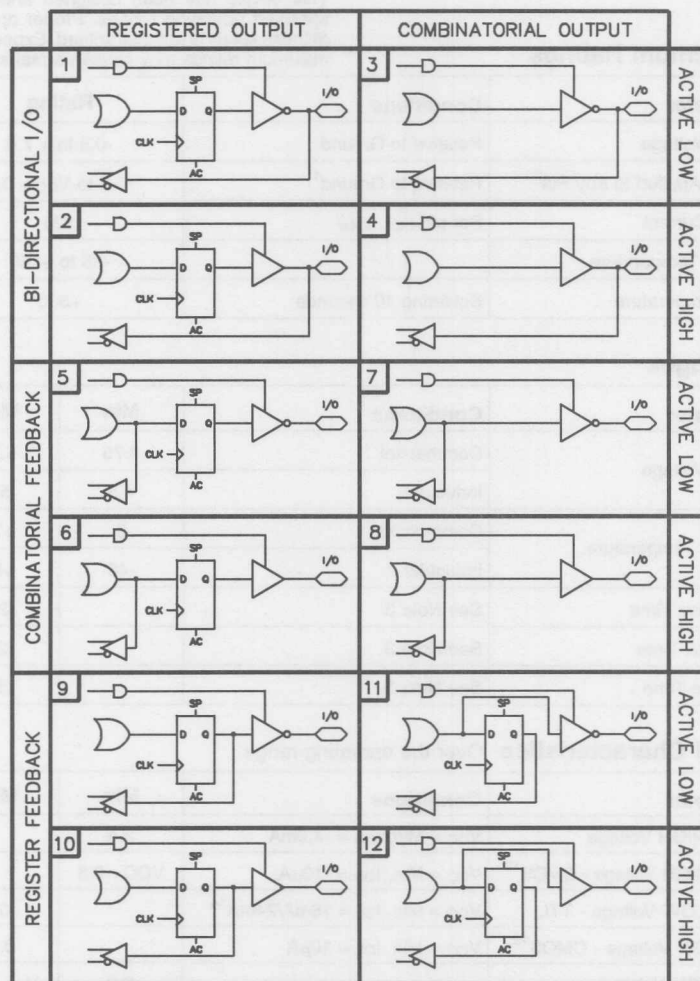


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL18CV8 I/O Macrocell.

#	Configuration				Input/Feedback Select	Output Select	
	A	B	C	D			
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1	"	"	Active High
3	1	0	1	1	"	Combinatorial	Active Low
4	0	0	1	1	"	"	Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0	"	"	Active High
7	1	0	1	0	"	Combinatorial	Active Low
8	0	0	1	0	"	"	Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0	"	"	Active High
11	1	0	0	0	"	Combinatorial	Active Low
12	0	0	0	0	"	"	Active High

Table 1. PEEL18CV8 Macrocell Configuration Bits

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T _A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T _R	Clock Rise Time	See Note 3		20	ns
T _F	Clock Fall Time	See Note 3		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 3		250	ms

D.C. Electrical Characteristics Over the operating range

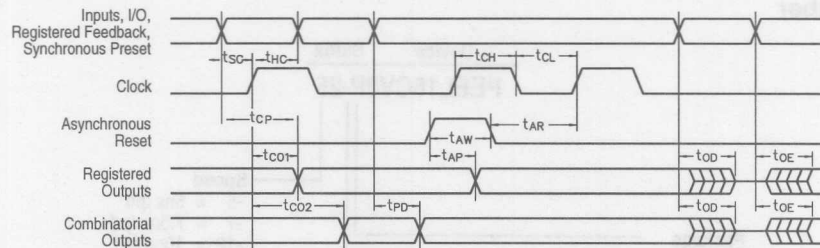
Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage - CMOS ¹³	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.3		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA/24mA ¹⁴		0.5	V
V _{OLc}	Input LOW Voltage - CMOS ¹³	V _{CC} = Min, I _{OL} = 10μA		0.15	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
I _{IL}	Input, I/O Leakage Current LOW	V _{CC} = Max, V _{IN} = GND	0 (Typ)	-10	μA
I _{IH}	Input, I/O Leakage Current HIGH	V _{CC} = Max, V _{IN} = V _{CC}	0 (Typ)	40	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5V, V _O = 0.5V ⁹ , T _A = 25°C	-30	-135	mA
I _{CC} ¹⁰	V _{CC} Current (See CR-1 for typical I _{CC})	V _{IN} = 0V or 3V f = 25MHz All outputs disabled ⁴	-5	90	mA
			-7	110	
			-10/-10	110/115	
			-15/-15	45/55	
			-25/-25	37/50	
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT} ⁷	Output Capacitance			12	pF

A.C. Electrical Characteristics

Over the Operating Range ^{8, 11}

Symbol	Parameter	-5		-7		-10 / I-10		-15 / I-15		-25 / I-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD}	Input ⁵ to non-registered output		5		7.5		10		15		25	ns
t _{OE}	Input ⁵ to output enable ⁶		5		7.5		10		15		25	ns
t _{OD}	Input ⁵ to output disable ⁶		5		7.5		10		15		25	ns
t _{CO1}	Clock to output		4		7		7		12		15	ns
t _{CO2}	Clock to comb. output delay via internal registered feedback		7.5		10		12		25		35	ns
t _{CF}	Clock to Feedback		2.5		3.5		4		8		15	ns
t _{SC}	Input ⁵ or feedback setup to clock	3.5		5		5		12		20		ns
t _{HC}	Input ⁵ hold after clock	0		0		0		0		0		ns
t _{CL} , t _{CH}	Clock low time, Clock high time ⁸	3		3.5		5		10		15		ns
t _{CP}	Min clock period, Ext (t _{SC} + t _{CO1})	7		12		12		24		35		ns
f _{MAX1}	Internal Feedback (1/t _{SC} +t _{CF}) ¹²	166.7		117.6		111		50		28.5		MHz
f _{MAX2}	External frequency External (1/t _{CP}) ¹²	133		83.3		83.3		41.6		28.5		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹²	166.7		142.8		100		50		33.3		MHz
t _{AW}	Asynchronous Reset pulse width	5		7.5		10		15		25		ns
t _{AP}	Input ⁵ to Asynchronous Reset		5		7.5		10		15		25	ns
t _{AR}	Asynchronous Reset Recovery Time		5		7.5		10		15		25	ns
t _{RESET}	Power-on reset time for registers in clear state		5		5		5		5		5	μs

Switching Waveforms



Notes

- Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
- V_I and V_O are not specified for program/verify operation.
- Test points for Clock and V_{CC} in t_r, t_f are referenced at 10% and 90% levels.
- I/O pins are 0V and 3V.
- "Input" refers to an Input pin signal.
- t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; V_{REF} = V_L see test loads in Section 6 of this Data Book.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- Test one output at a time for a duration of less than 1 sec.
- ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
- PEEL Device test loads are specified in Section 6 of this Data Book.
- Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
- Available only for 18CV8 -7/10/I-10/15/I-15/25/I-25 grades.
- 24mA available for 18CV8-5, all other speeds are 16mA.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL18CV8J-5	5ns	C	J20
PEEL18CV8P-7	7.5ns	C	P20
PEEL18CV8J-7	7.5ns	C	J20
PEEL18CV8S-7	7.5ns	C	S20
PEEL18CV8P-10	10ns	C	P20
PEEL18CV8PI-10		I	
PEEL18CV8J-10	10ns	C	J20
PEEL18CV8JI-10		I	
PEEL18CV8S-10	10ns	C	S20
PEEL18CV8SI-10		I	
PEEL18CV8T-10	10ns	C	T20
PEEL18CV8TI-10		I	
PEEL18CV8P-15	15ns	C	P20
PEEL18CV8PI-15		I	
PEEL18CV8J-15	15ns	C	J20
PEEL18CV8JI-15		I	
PEEL18CV8S-15	15ns	C	S20
PEEL18CV8SI-15		I	
PEEL18CV8T-15	15ns	C	T20
PEEL18CV8TI-15		I	
PEEL18CV8P-25	25ns	C	P20
PEEL18CV8PI-25		I	
PEEL18CV8J-25	25ns	C	J20
PEEL18CV8JI-25		I	
PEEL18CV8S-25	25ns	C	S20
PEEL18CV8SI-25		I	
PEEL18CV8T-25	25ns	C	T20
PEEL18CV8TI-25		I	

Contact ICT for availability of -5 / -7 speed grades in TSSOP packages.

Part Number

Device Suffix
PEEL18CV8P-25

Package

P = Plastic 300mil DIP
J = Plastic (J) Leaded Chip Carrier (PLCC)
S = SOIC
T = TSSOP

Speed

-5 = 5ns tpd
-7 = 7.5ns tpd
-10 = 10ns tpd
-15 = 15ns tpd
-25 = 25ns tpd

Temperature Range

(Blank) = Commercial 0 to +70°C
I = Industrial -40 to +85°C

PEEL™ 20V8 -5/-7/-10/-15/-25 CMOS Programmable Electrically Erasable Logic

Features

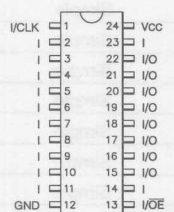
- **Compatible with Popular 20V8 Devices**
 - 20V8 socket and function compatible
 - Programs with standard 20V8 JEDEC file
 - 24-pin DIP/SOIC, 28-pin PLCC packages
- **CMOS Electrically Erasable Technology**
 - Superior factory testing
 - Reprogrammable in plastic package
 - Reduces retrofit and development costs
- **Application Versatility**
 - Replaces random logic
 - Super-sets standard 24-pin PLDs (PALs)
- **Low Power and Quarter Power Versions**
 - Low Power: 75mA typical I_{CC}
 - Quarter Power: 45mA typical I_{CC}
- **Development/Programmer Support**
 - Third party software and programmers
 - ICT PLACE Development Software and PDS-3 programmer
 - Automatic programmer translation and JEDEC file translation software available for the most popular PAL devices

General Description

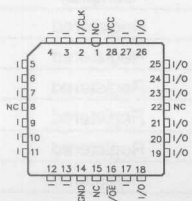
The PEEL20V8 is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL20V8 offers the performance, flexibility, ease-of-design and production practicality needed by logic designers today. The PEEL20V8 is available in 24-pin DIP, PLCC and SOIC packages (see Figure 1) with speeds ranging from 5ns to 25ns and power consumption as low as 45mA. EE-reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-reprogrammability also improves fac-

tory testability, thus ensuring the highest quality possible. The PEEL20V8 is socket and function compatible with other 20V8 devices. Its architecture allows it to replace many standard 24-pin PALs. See Figure 2. ICT's PEEL20V8 can be programmed with any existing 20V8 JEDEC file. Some programmers also allow the PEEL20V8 to be programmed directly from PAL 20L8, 20R4, 20R6 and 20R8 JEDEC files. Additional development and programming support for the PEEL20V8 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

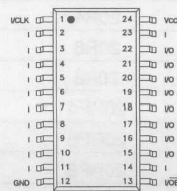
Pin Configuration (Figure 1)



DIP

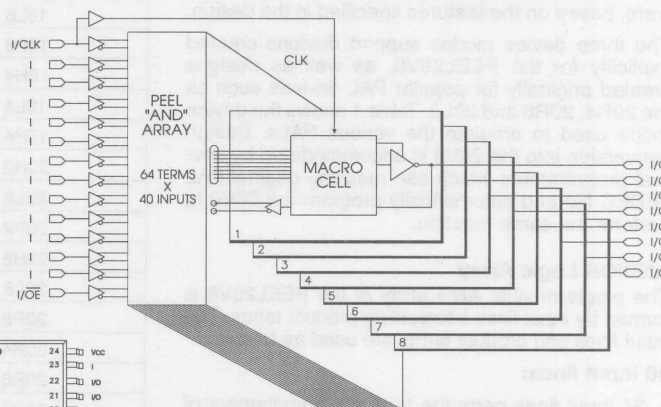


PLCC



SOIC

Block Diagram (Figure 2)



Functional Description

The PEEL20V8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of macrocells further increase logic flexibility.

Architecture Overview

The PEEL20V8 features fourteen dedicated input pins and eight I/O pins, which allow a total of up to 20 inputs and 8 outputs for creating logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL20V8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the eight OR functions is a macrocell which can be independently programmed to one of up to four different basic configurations: active-high or active-low registered logic output (with registered feedback) or active-high or active-low combinatorial logic output (with I/O pin feedback).

Three different device modes, Simple, Complex and Registered, support various user configurations. In Simple mode a macrocell can be configured for combinatorial function with the output buffer permanently enabled, or the output buffer can be disabled and the I/O pin used as a dedicated input. In Complex mode a macrocell is configured for combinatorial function with the output buffer enable controlled by a product term. In Registered mode, a macrocell can be configured for registered operation with the register clock and output buffer enable controlled directly from pins, or can be configured for combinatorial function with the output buffer enable controlled by a product term. In most cases the device mode is set automatically by the development software, based on the features specified in the design.

The three device modes support designs created explicitly for the PEEL20V8, as well as designs created originally for popular PAL devices such as the 20R4, 20R8 and 20L8. Table 1 shows the device mode used to emulate the various PALs. Design conversion into the 20V8 is accommodated by several programmers which can read the original PAL JEDEC file and automatically program the 20V8 to perform the same function.

AND/OR Logic Array

The programmable AND array of the PEEL20V8 is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

40 input lines:

24 input lines carry the true and complement of the signals applied to the 12 dedicated input pins

16 additional lines carry the true and complement of 8 macrocell feedback signals or inputs from I/O pins or the clock/OE pins

64 product terms:

56 product terms (arranged in 8 groups of 7) form sum-of-product functions for macrocell combinatorial or registered logic

8 product terms (arranged 1 per macrocell) add an additional product term for macrocell sum-of-products functions or I/O pin output enable control

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 32-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, that term will always be TRUE.

When programming the PEEL20V8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program at least one pair of complementary inputs on unused product terms so that they will have no effect on the output function.)

Table 1. PEEL20V8/PAL Device Compatibility

PAL Architecture Compatibility	PEEL20V8 Device Mode
14H8	Simple
14L8	Simple
14P8	Simple
16H6	Simple
16L6	Simple
16P6	Simple
18H4	Simple
18L4	Simple
18P4	Simple
20H2	Simple
20L2	Simple
20P2	Simple
20H8	Complex
20L8	Complex
20P8	Complex
20R4	Registered
20R6	Registered
20R8	Registered
20RP4	Registered
20RP6	Registered
20RP8	Registered

Programmable Macrocell

The macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20V8 to the precise requirements of their designs.

Macrocell Architecture

Each macrocell consists of an OR function, a D-type flip-flop, an output polarity selector, and a programmable feedback path. Four EEPROM architecture bits MS0, MS1, OP and RC control the configuration of each macrocell. Bits MS0 and MS1 are global, and select between Simple, Complex, and Registered mode for the whole device. Bits OP and RC are local for each macrocell; bit OP controls the output polarity and bit RC selects between registered and combinatorial operation and also specifies the feedback path. Table 2 shows the architecture bit settings for each possible configuration.

Equivalent circuits for the possible macrocell configurations are illustrated in Figures 3, 4 and 5. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Simple Mode

In Simple mode, all eight product terms feed the OR array which can generate a purely combinatorial function for the output pin. The programmable output polarity selector allows active-high or active-low logic, eliminating the need for external inverters. For output functions, the buffer can be permanently enabled. Feedback into the array is available on all

macrocell I/O pins, except for DIP/SOIC pins 18 and 19 (PLCC pins 21 and 23). Figure 6 shows the logic array of the PEEL20V8 configured in Simple mode.

Simple mode also provides the option of configuring an I/O pin as a dedicated input. In this case the output buffer is permanently disabled, and the I/O pin feedback is used to bring the input signal from the pin into the logic array. This option is available for all I/O pins except pins 18 and 19 (PLCC pins 21 and 23).

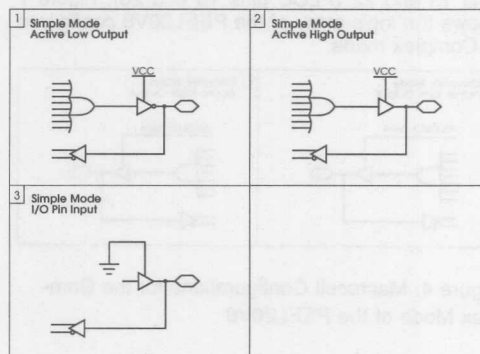


Figure 3. Macrocell Configurations for the Simple Mode of the PEEL20V8

Table 2. PEEL20V8 Device Mode/Macrocell Configuration Bits

Config. #	Mode	Architecture Bits				Function	Polarity	Feedback
		MS0	MS1	OP	RC			
1	Simple	1	0	0	0	Combinatorial	Active Low	I/O Pin
2	Simple	1	0	1	0	Combinatorial	Active High	I/O Pin
3	Simple	1	0	X	1	None	None	I/O Pin
1	Complex	1	1	0	1	Combinatorial	Active Low	I/O Pin
2	Complex	1	1	1	1	Combinatorial	Active High	I/O Pin
1	Registered	0	1	0	0	Registered	Active Low	Registered
2	Registered	0	1	1	0	Registered	Active High	Registered
3	Registered	0	1	0	1	Combinatorial	Active Low	I/O Pin
4	Registered	0	1	1	1	Combinatorial	Active High	I/O Pin

Complex Mode

In Complex mode, seven product terms feed the OR array which can generate a purely combinational function for the output pin. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. The output buffer is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all pins except DIP/SOIC pins 15 and 22 (PLCC pins 18 and 26). Figure 7 shows the logic array of the PEEL20V8 configured in Complex mode.

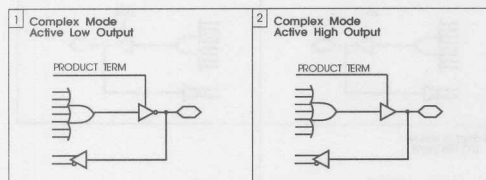


Figure 4. Macrocell Configurations for the Complex Mode of the PEEL20V8

Registered Mode

Registered mode provides eight product terms to the OR array for registered functions. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. (Note, however, that PEEL20V8 registers power-up reset and so before the first clock arrives the output at the pin will be low if the user has selected active-high logic and high if the user has selected active-low logic.) For registered functions, the output buffer enable is controlled directly from the /OE control pin. Feedback into the array comes from the macrocell register. In Registered mode, DIP/SOIC input pins 1 and 13 (PLCC pins 2 and 16) are permanently allocated as CLK and /OE, respectively. Figure 8 shows the logic array of the PEEL20V8 configured in Registered mode.

Registered mode also provides the option of configuring a macrocell for combinational operation, with seven product terms feeding the OR function.

Again the programmable output polarity selector provides active-high or active-low logic. The output buffer enable is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all I/O pins.

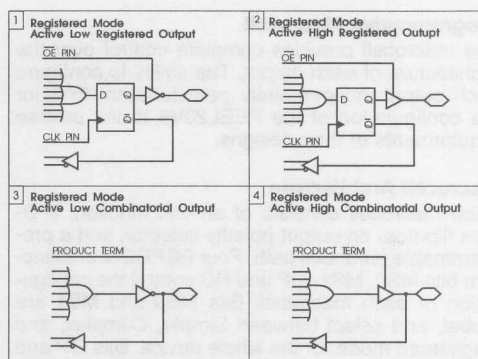


Figure 5. Macrocell Configurations for the Registered Mode of the PEEL20V8

Input and I/O Pin Pull-ups

The input and I/O pins on this device feature pull-up circuitry. The pull-ups cause input and I/O pins to be pulled high through nominally 100k ohms.

Design Security

The PEEL20V8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit has been set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL20V8. The code cannot be read back after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

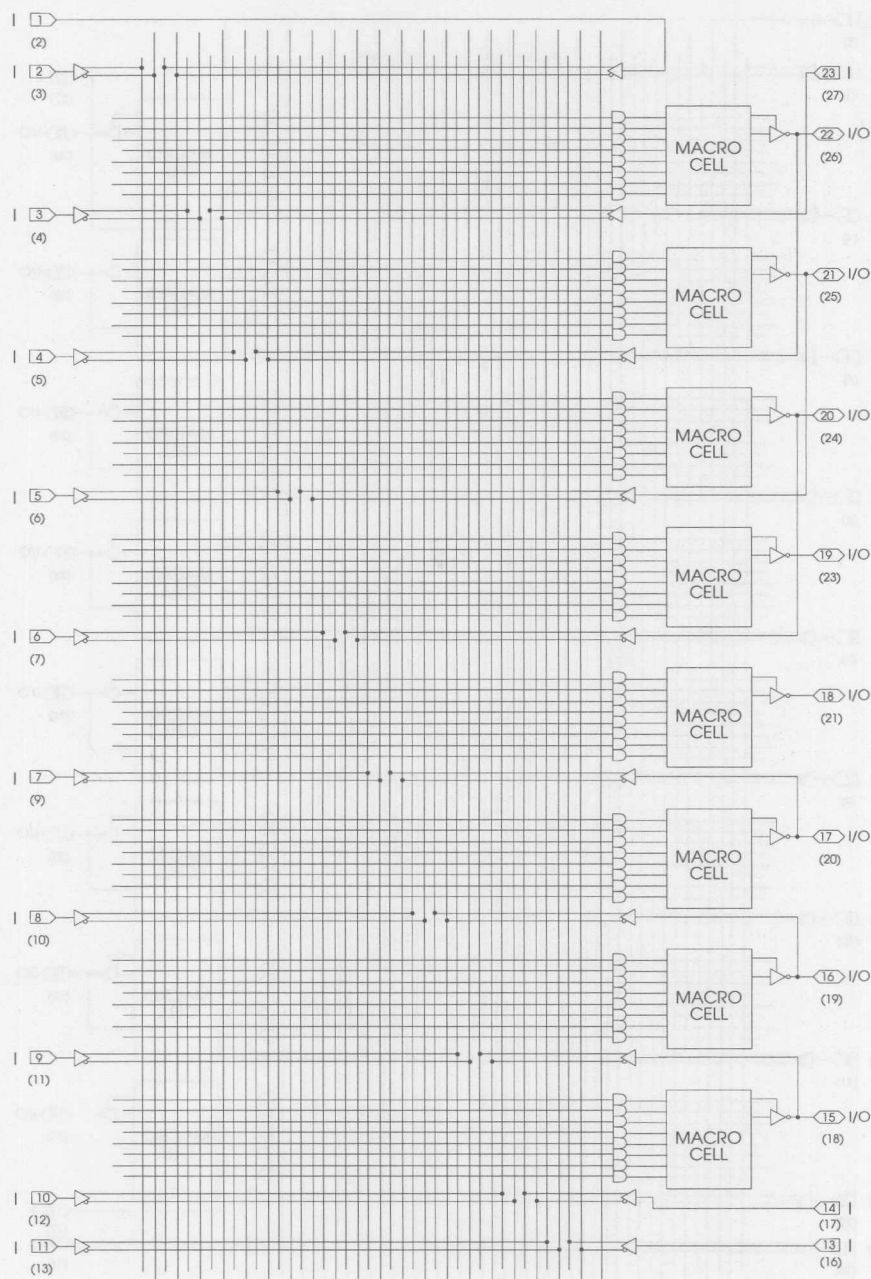


Figure 6. PEEL20V8 Logic Array - Simple Mode
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

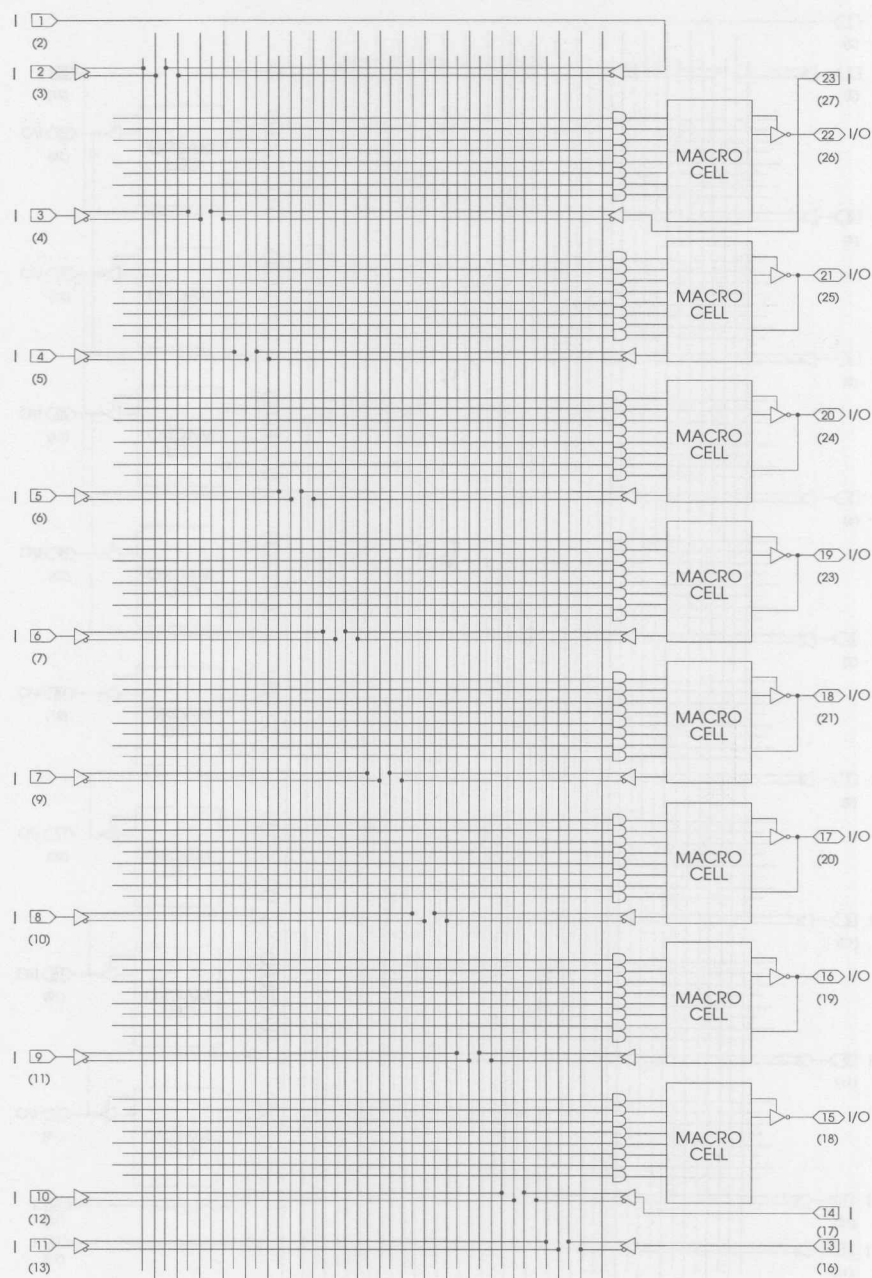


Figure 7. PEEL20V8 Logic Array - Complex Mode
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

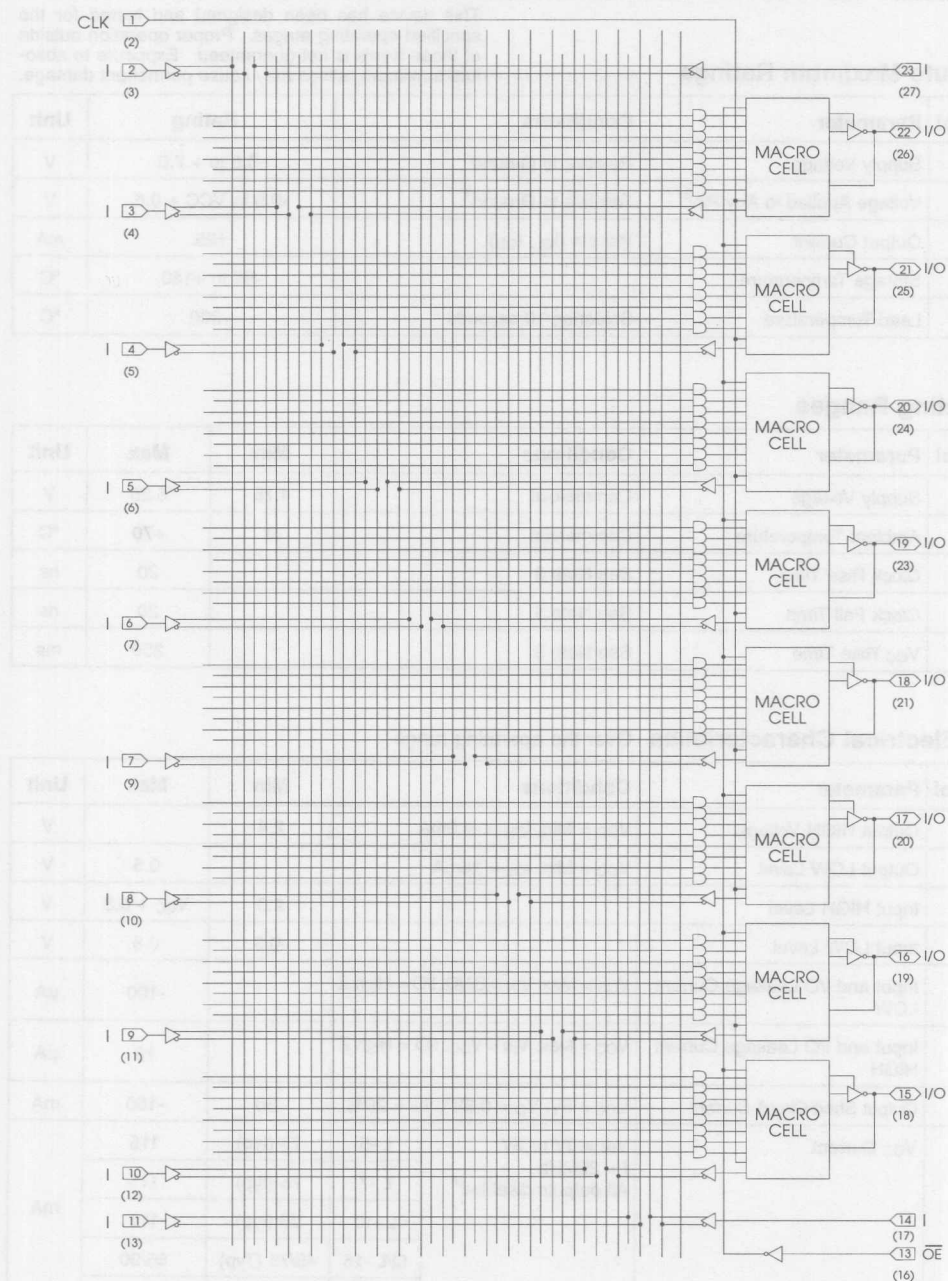


Figure 8. PEEL20V8 Logic Array - Registered Mode
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
T _A	Ambient Temperature	Commercial	0	+70	°C
T _R	Clock Rise Time	See Note 3		20	ns
T _F	Clock Fall Time	See Note 3		20	ns
TRVCC	V _{CC} Rise Time	See Note 3		250	ms

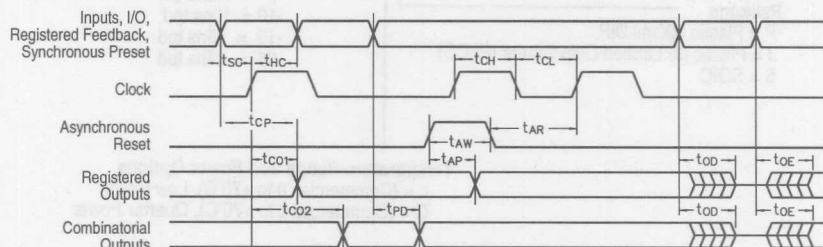
D.C. Electrical Characteristics Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OL}	Output LOW Level	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		-0.3	0.8	V
I _{IL}	Input and I/O Leakage Current LOW	V _{CC} = Max, V _{IN} = GND, I/O = High Z		-100	μA
I _{IH}	Input and I/O Leakage Current HIGH	V _{CC} = Max, V _{IN} = V _{CC} , I/O = High Z		10	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5V, V _O = 0.5V ⁹ , T _A = 25°C	-30	-150	mA
I _{CC} ¹⁰	V _{CC} Current	V _{IN} = 0V or 3V f = 25MHz All outputs disabled ⁴	L -5	75 (typ)	mA
			L -7	75 (typ)	
			L -10	75 (typ)	
			Q/L -15	45/75 (Typ)	
			Q/L -25	45/75 (Typ)	
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT} ⁷	Output Capacitance			12	pF

A.C. Electrical Characteristics

 Over the Operating Range ^{8, 11}

Symbol	Parameter	L-5		L-7		L-10		Q/L-15		Q/L-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD}	Input ⁵ to non-registered output	1	5	3	7.5	3	10	3	15	3	25	ns
t _{OE}	Input ⁵ to output enable ⁶	1	5	3	7.5		10		15		20	ns
t _{OD}	Input ⁵ to output disable ⁶	1	5	3	7.5		10		15		20	ns
t _{CO1}	Clock to output	1	4		7	2	7	2	10	2	12	ns
t _{CO2}	Clock to comb. output delay via internal registered feedback		7.5		10		12		25		35	ns
t _{CF}	Clock to Feedback		3		3.5		4		8		10	ns
t _{SC}	Input ⁵ or feedback setup to clock	3		5		5		12		15		ns
t _{HC}	Input ⁵ hold after clock	0		0		0		0		0		ns
t _{CL} , t _{CH}	Clock low time, clock high time ⁸	3		3.5		5		8		12		ns
t _{CP}	Min clock period Ext (t _{SC} + t _{CO1})	7		12		12		22		27		ns
f _{MAX1}	Internal Feedback (1/t _{SC} +t _{CF}) ¹²	166.6		117.6		111.1		50		40		MHz
f _{MAX2}	External Feedback (1/t _{CP}) ¹²	142.8		83.3		83.3		45.5		37		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹²	166.6		142.8		100		62.5		41.6		MHz
t _{AW}	Asynchronous Reset pulse width	5		7.5		10		15		25		ns
t _{AP}	Input ⁵ to Asynchronous Reset		5		7.5		10		15		25	ns
t _{AR}	Asynchronous Reset recovery time		5		7.5		10		15		25	ns
t _{RESET}	Power-on reset time for registers in clear state						5		5		5	μs

Switching Waveforms

Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_r, t_f are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. "Input" refers to an Input pin signal.
6. t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; V_{REF} = V_L see test loads in Section 6 of this Data Book.
7. Capacitances are tested on a sample basis.

8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration of less than 1 sec.
10. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
11. PEEL Device test loads are specified in Section 6 of this Data Book.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL20V8JL-5*	5ns	C	J28
PEEL20V8PL-7*	7.5ns	C	P24
PEEL20V8JL-7*	7.5ns	C	J28
PEEL20V8SL-7*	7.5ns	C	S24
PEEL20V8PL-10*	10ns	C	P24
PEEL20V8JL-10*	10ns	C	J28
PEEL20V8SL-10*	10ns	C	S24
PEEL20V8PL-15	15ns	C	P24
PEEL20V8PQ-15		C	
PEEL20V8JL-15	15ns	C	J28
PEEL20V8JQ-15		C	
PEEL20V8SL-15	15ns	C	S24
PEEL20V8SQ-15		C	
PEEL20V8PL-25	25ns	C	P24
PEEL20V8PQ-25		C	
PEEL20V8JL-25	25ns	C	J28
PEEL20V8JQ-25		C	
PEEL20V8SL-25	25ns	C	S24
PEEL20V8SQ-25		C	

* Contact ICT for availability of the -5, -7 and -10 speed grades.

Device Suffix
PEEL20V8PL-25

Package

P = Plastic 300mil DIP
J = Plastic (J) Leadless Chip Carrier (PLCC)
S = SOIC

Speed

-5 = 5ns tpd
-7 = 7.5ns tpd
-10 = 10ns tpd
-15 = 15ns tpd
-25 = 25ns tpd

Temperature Range and Power Options

L = (Commercial 0 to +70°C), Low Power
Q = (Commercial 0 to +70°C), Quarter Power

PEEL™ 22CV8 -5/-7/-10/-15/-25 **CMOS Programmable Electrically Erasable Logic Device**

Features

■ High Speed, Low Power

- 5, 7, 10, 15, 25ns tpd speed grades
- Less power than quarter-power PALs and GALs

■ CMOS Electrically Erasable Technology

- Superior factory testing
- Reprogrammable in plastic package
- Reduces retrofit and development costs

■ Development/Programmer Support

- Third party software and programmers
- ICT PLACE Development Software and PDS-3 programmer

■ Architectural Flexibility

- 24-pin version of popular PEEL18CV8
- 74 product term x 44 input array
- Up to 22 inputs and 8 I/O pins
- Up to 12 configurations per macrocell
- Synchronous preset, asynchronous clear
- Individual product-term driven OE controls

■ Application Versatility

- Replaces random logic
- Super-sets standard PLDs (PAL, GAL, EPLD)
- Enhanced architecture fits more logic than ordinary PLDs
- 24-pin DIP/SOIC/TSSOP, 28-pin PLCC

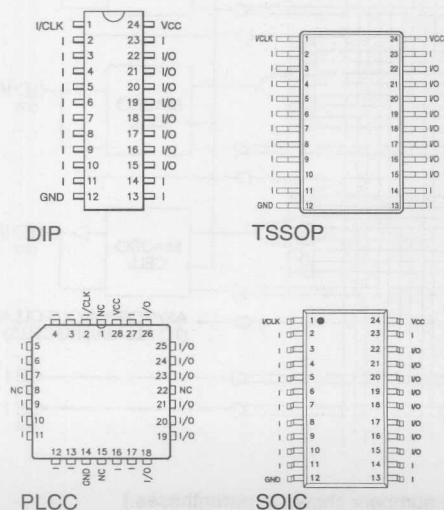
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General Description

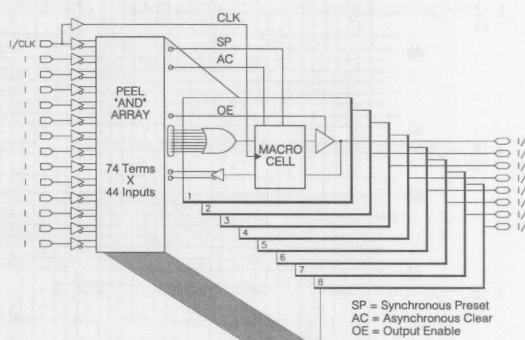
The PEEL22CV8 is a Programmable Electrically Erasable Logic (PEEL) device providing an architecture-enhanced low power alternative to ordinary PLDs such as the GAL20V8. The PEEL22CV8 is available in 24-pin DIP/SOIC/TSSOP, and 28-pin PLCC packages with speeds ranging from 5ns to 25ns (the 5ns speed grade is available only in the PLCC package). The low power consumption of this device (10mA typical for the 25ns speed grade) makes it ideal for power-sensitive applications such as portable communication equipment, computers and peripherals. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable pro-

duction inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability, thus ensuring the highest quality possible. The PEEL22CV8 architecture allows it to replace over 20 standard 24-pin PLDs (PAL, GAL, EPLD, etc.), often at less than half of the power of a quarter power GAL. The device also provides additional architecture features so more logic can be put into every design. Development and programming support for the PEEL22CV8 is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



Block Diagram (Figure 2)



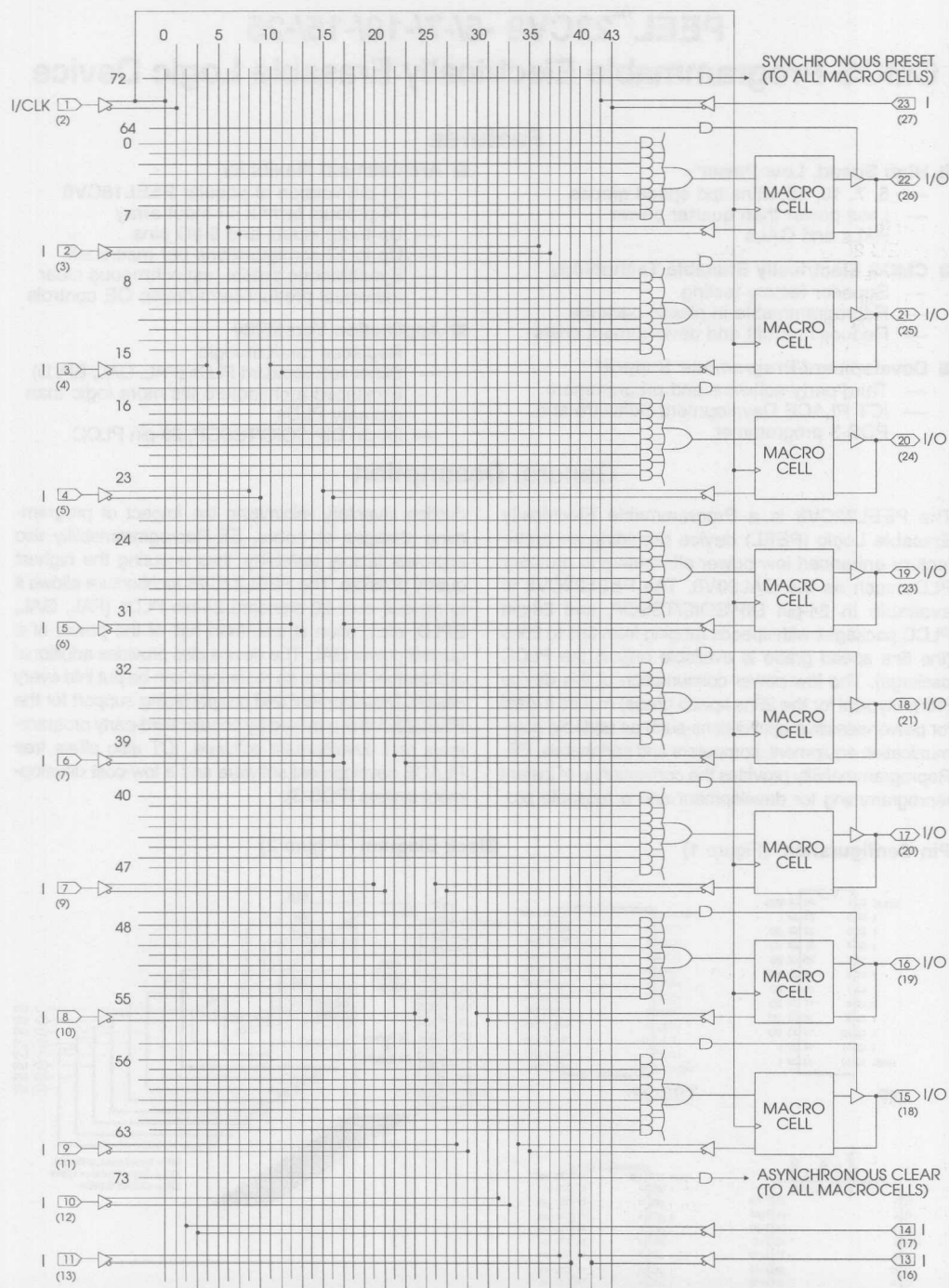


Figure 3. PEEL22CV8 Logic Array Diagram

(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

Function Description

The PEEL22CV8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL22CV8 architecture is illustrated in the block diagram of Figure 2. Fourteen dedicated inputs and eight I/Os provide up to 22 inputs and 8 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL22CV8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the 8 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL22CV8 (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 28 input lines carry the true and complement of the signals applied to the 14 input pins

- 16 additional lines carry the true and complement values of feedback or input signals from the 8 I/Os

74 product terms:

- 64 product terms (arranged in groups of 8) used to form sum of product functions

- 8 output enable terms (one for each I/O)

- 1 global synchronous preset term

- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections

on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL22CV8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program at least one pair of complementary inputs on unused product terms so that they will have no effect on the output function.)

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV8 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Refer to Table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9 and 10) the macrocell provides eight additional configurations. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or clocked into the D-type flip-flop (registered function). The D-type flip-flop loads data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if at least one complementary pair of connections is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL22CV8 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output of the OR gate, bypassing the output buffer, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7 and 8 in Figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing combinatorial output functions, registered feedback allows internal registering of states without giving up the use of the external output.

Programmable Input and I/O Pin Pull-ups

The input and I/O pins on this device feature programmable pull-up circuitry which can be globally enabled or disabled during design entry. (In the ICT PLACE software, for example, the pull-ups can be activated by selecting the Design...Auxiliary menu, the default is no pull-ups.) Enabling the pull-ups causes input and I/O pins to be pulled high through nominally 100k ohms.

Design Security

The PEEL22CV8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

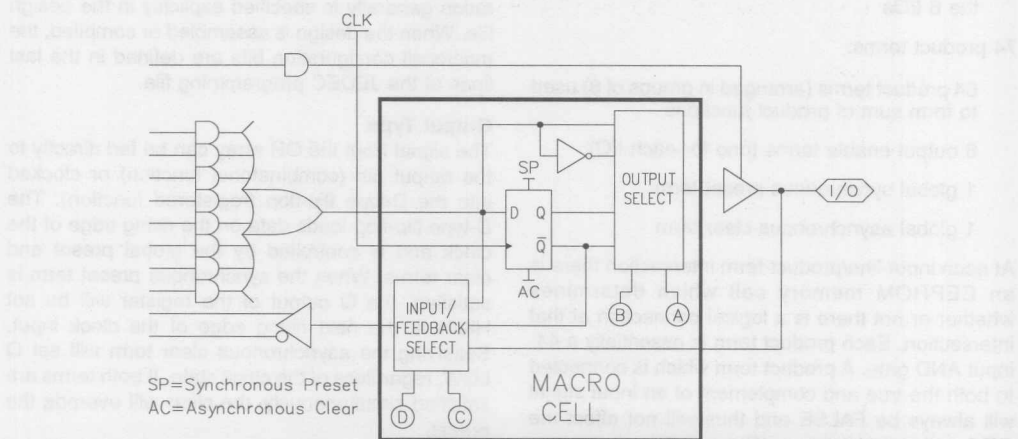


Figure 4. Block Diagram of The PEEL22CV8 I/O Macrocell

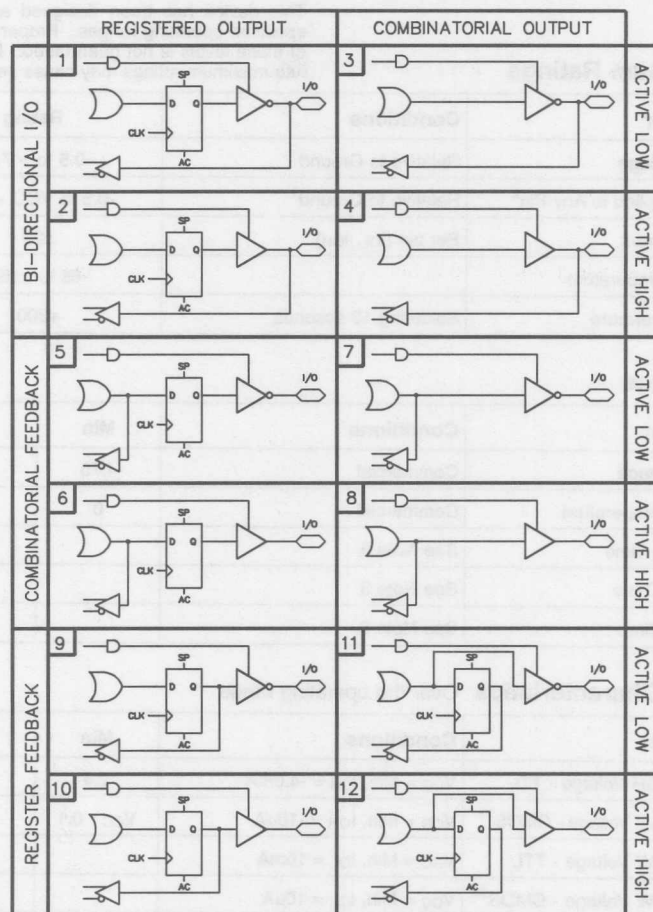


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL22CV8 I/O Macrocell

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1	"	"	Active High
3	1	0	1	1	"	Combinatorial	Active Low
4	0	0	1	1	"	"	Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0	"	"	Active High
7	1	0	1	0	"	Combinatorial	Active Low
8	0	0	1	0	"	"	Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0	"	"	Active High
11	1	0	0	0	"	Combinatorial	Active Low

Table 1. PEEL22CV8 Macrocell Configuration Bits

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
T _A	Ambient Temperature	Commercial	0	+70	°C
T _R	Clock Rise Time	See Note 3		20	ns
T _F	Clock Fall Time	See Note 3		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 3		250	ms

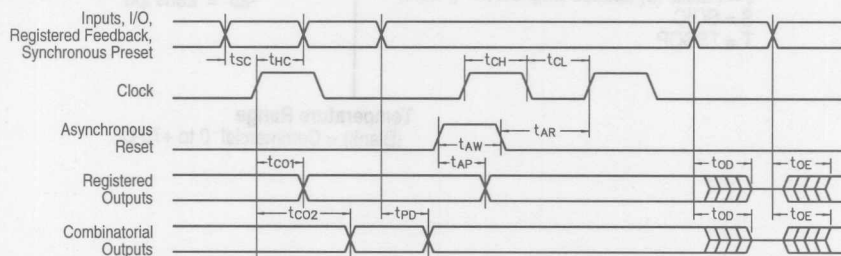
D.C. Electrical Characteristics Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage - CMOS ¹³	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{OLc}	Output LOW Voltage - CMOS ¹³	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		-0.3	0.8	V
I _{IL}	Input, I/O Leakage Current LOW-Input and I/O pull-ups disabled	V _{CC} = Max, V _{IN} = GND, I/O = High Z		-10	μA
I _{ILP}	Input, I/O Leakage Current LOW-Input and I/O pull-ups enabled	V _{CC} = Max, V _{IN} = GND, I/O = High Z		-100	μA
I _{IH}	Input, I/O Leakage Current HIGH	V _{CC} = Max, V _{IN} = V _{CC} , I/O = High Z		10	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5V, V _O = 0.5V ⁹ , T _A = 25°C	-30	-150	mA
I _{CC} ¹⁰	V _{CC} Current	V _{IN} = 0V or 3V f = 25MHz All outputs disabled ⁴	-5	75 (Typ)	mA
			-7	60 (Typ)	
			-10	60 (Typ)	
			-15	20 (Typ)	
			-25	10 (Typ)	
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT} ⁷	Output Capacitance			12	pF

A.C. Electrical Characteristics

 Over the Operating Range ^{8, 11}

Symbol	Parameter	-5		-7		-10		-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD}	Input ⁵ to non-registered output		5		7.5		10		15		25	ns
t _{OE}	Input ⁵ to output enable ⁶		5		7.5		10		15		20	ns
t _{OD}	Input ⁵ to output disable ⁶		5		7.5		10		15		20	ns
t _{CO1}	Clock to output		4		7		7		10		12	ns
t _{CO2}	Clock to comb. output delay via internal registered feedback		7.5		10		12		20		30	ns
t _{CF}	Clock to Feedback		2.5		3.5		4		8		10	ns
t _{SC}	Input ⁵ or feedback setup to clock	3.5		5		5		10		15		ns
t _{HC}	Input ⁵ hold after clock	0		0		0		0		0		ns
t _{CL} , t _{CH}	Clock low time, clock high time ⁸	3		3.5		5		8		12		ns
t _{CP}	Min clock period Ext (t _{SC} + t _{CO1})	7.5		12		12		20		27		ns
f _{MAX1}	Internal Feedback (1/t _{SC} +t _{CF}) ¹²	166.7		117.6		111		55.6		40		MHz
f _{MAX2}	External Feedback (1/t _{CP}) ¹²	133		83.3		83.3		50		37		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹²	166.7		142.8		100		62.5		41.6		MHz
t _{AW}	Asynchronous Reset pulse width	5		7.5		10		15		25		ns
t _{AP}	Input ⁵ to Asynchronous Reset		5		7.5		10		15		25	ns
t _{AR}	Asynchronous Reset recovery time		5		7.5		10		15		25	ns
t _{RESET}	Power-on reset time for registers in clear state		5		5		10		5		5	μs

Switching Waveforms

Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
4. I/O pins are 0V or 3V.
5. "Input" refers to an Input pin signal.
6. t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; V_{REF} = V_I see test loads in Section 6 of this Data Book.
7. Capacitances are tested on a sample basis.

8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration of less than 1 sec.
10. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
11. PEEL Device test loads are specified in Section 6 of this Data Book.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
13. Available only for 22CV8 -15/-25 speed grades.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL22CV8J-5*	5ns	C	J28
PEEL22CV8P-7*	7.5ns	C	P24
PEEL22CV8J-7*	7.5ns	C	J28
PEEL22CV8S-7*	7.5ns	C	S24
PEEL22CV8P-10*	10ns	C	P24
PEEL22CV8J-10*	10ns	C	J28
PEEL22CV8S-10*	10ns	C	S24
PEEL22CV8P-15	15ns	C	P24
PEEL22CV8J-15	15ns	C	J28
PEEL22CV8S-15	15ns	C	S24
PEEL22CV8P-25	25ns	C	P24
PEEL22CV8J-25	25ns	C	J28
PEEL22CV8S-25	25ns	C	S24

* Contact ICT for availability of this device in -5, -7 and -10 speed grades, as well as all speed grades in TSSOP packages.

Part Number

Device Suffix
PEEL22CV8P-25

Package

P = Plastic 300mil DIP
J = Plastic (J) Leaded Chip Carrier (PLCC)
S = SOIC
T = TSSOP

Speed

-5 = 5ns tpd
-7 = 7.5ns tpd
-10 = 10ns tpd
-15 = 15ns tpd
-25 = 25ns tpd

Temperature Range

(Blank) = Commercial 0 to +70°C

PEEL™ 20CG10A -5/-7/-10/-15/L-15/-25 **CMOS Programmable Electrically Erasable Logic**

Features

■ High Speed/Low Power

- Speeds ranging from 5ns to 25ns
- Power as low as 67mA at 25MHz

■ Electrically Erasable Technology

- Superior factory testing
- Reprogrammable in plastic package
- Reduces retrofit and development costs

■ Development/Programmer Support

- Third party software and programmers
- ICT Place Development Software and PDS-3 programmer
- PLD-to-PEEL JEDEC file translator

■ Architectural Flexibility

- 92 product term X 44 input AND array
- Up to 22 inputs and 10 outputs
- Up to 12 configurations per macrocell
- Synchronous preset, asynchronous clear
- Independent output enables
- 24-pin DIP, SOIC and 28-pin PLCC packages

■ Application Versatility

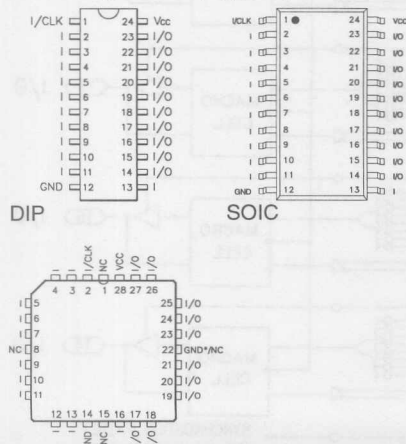
- Replaces random logic
- Super-sets standard PLDs (PAL, GAL, EPLD)
- Enhanced Architecture fits more logic than ordinary PLDs

General Description

The PEEL20CG10A is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL20CG10A offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL20CG10A is available in 24-pin DIP, SOIC and 28-pin PLCC packages with speeds ranging from 5ns to 25ns with power consumption as low as 67mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogram-

mability also improves factory testability thus, ensuring the highest quality possible. The PEEL20CG10A architecture allows it to replace over 20 standard 24-pin PLDs (PAL, GAL, EPLD etc.). It also provides additional architecture features so more logic can be put into every design. ICT's JEDEC file translator instantly converts existing 24-pin PLDs to the PEEL20CG10A without the need to rework the existing design. Development and programming support for the PEEL20CG10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

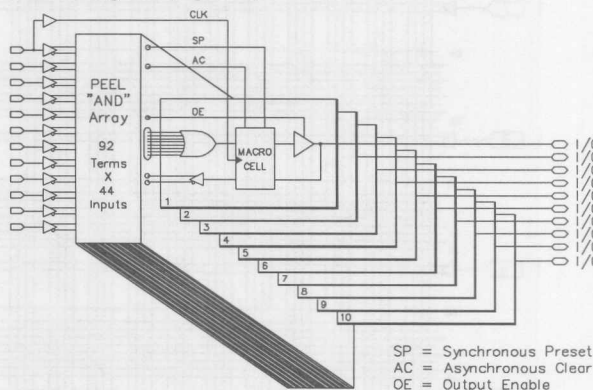
Pin Configuration (Figure 1)



*Optional extra ground pin for -5 speed grade.

PLCC

Block Diagram (Figure 2)



SP = Synchronous Preset
AC = Asynchronous Clear
OE = Output Enable

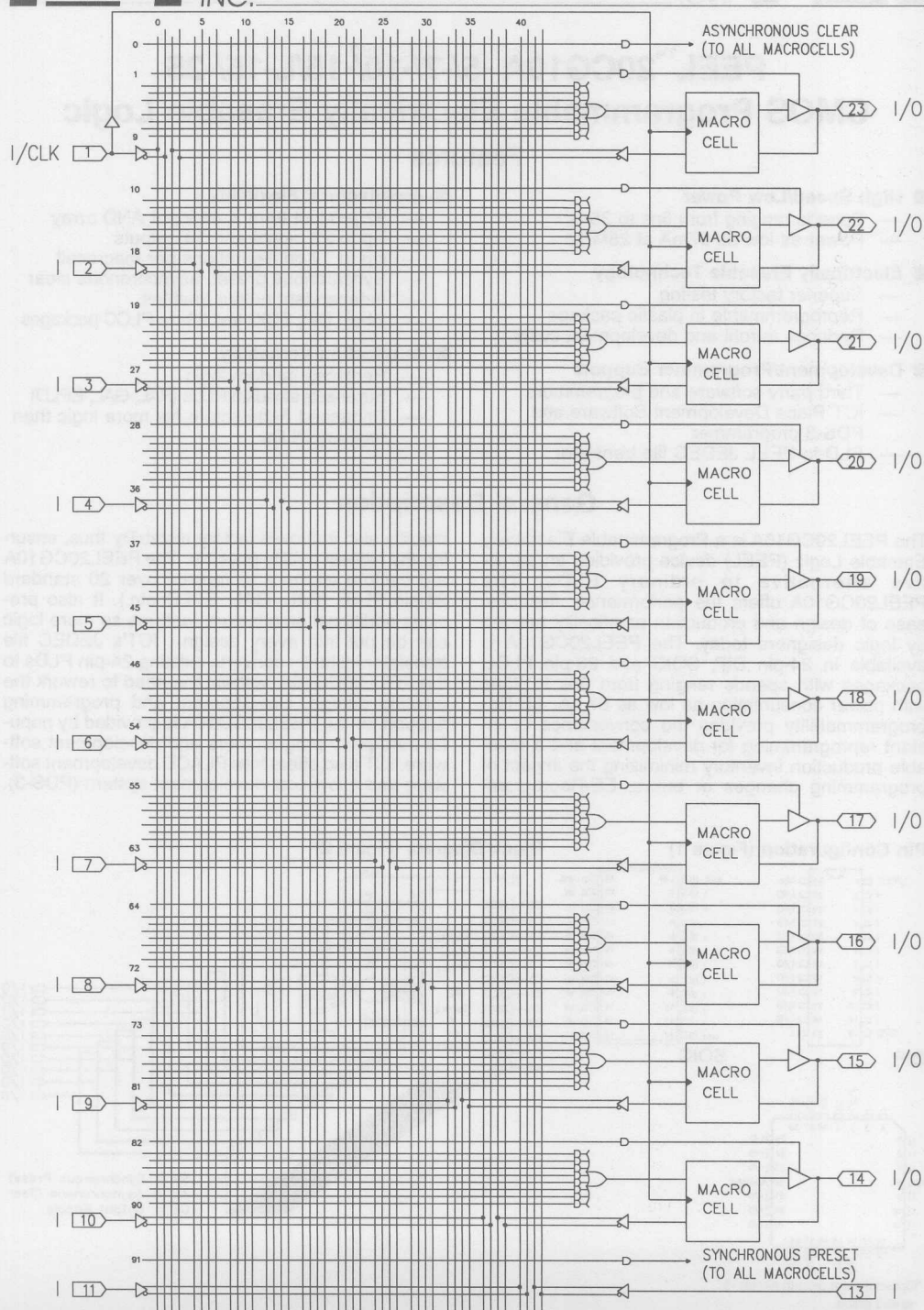


Figure 3. PEEL20CG10A Logic Array Diagram

Function Description

The PEEL20CG10A implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL20CG10A architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL20CG10A can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL20CG10A (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

92 product terms:

- 80 product terms (8 per I/O)
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE.

When programming the PEEL20CG10A, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every

logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function).

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20CG10A to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine: output polarity; output type (registered or non-registered); and input/feedback path (bi-directional I/O, combinatorial feedback, or register feedback). Table 1 shows the bit settings for each of the twelve macro-cell configurations.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 5. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10) the macrocell provides eight configurations that are unavailable in any PAL device.

Output Type

The signal from the OR array can be fed directly to the output pin or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL20CG10A macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O); directly from the Q output of the flip-flop (registered feedback); or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output directly from the

OR gate, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7 and 8 in Figure 5.)

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinatorial or registered. When implementing configurations 11 and 12 in Figure 5, the register can be used for internal latching of data while leaving the external output free for combinatorial functions.

Design Security

The PEEL20CG10A provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

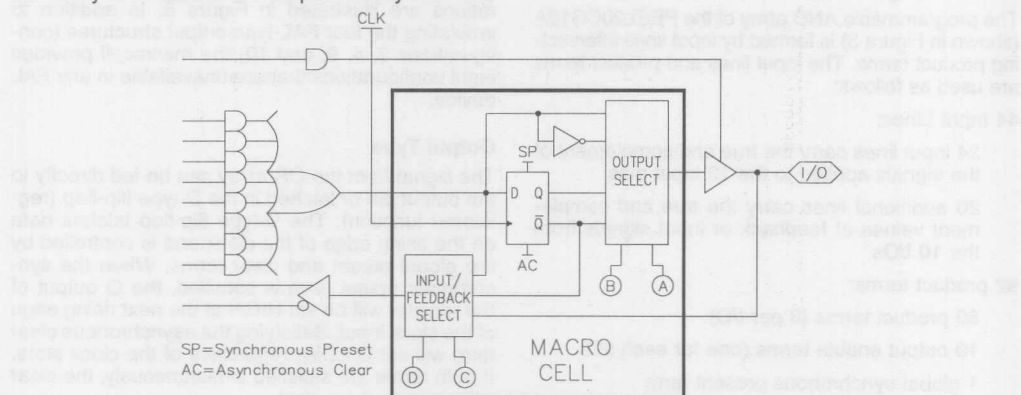


Figure 4. Block Diagram of the PEEL20CG10A I/O Macrocell

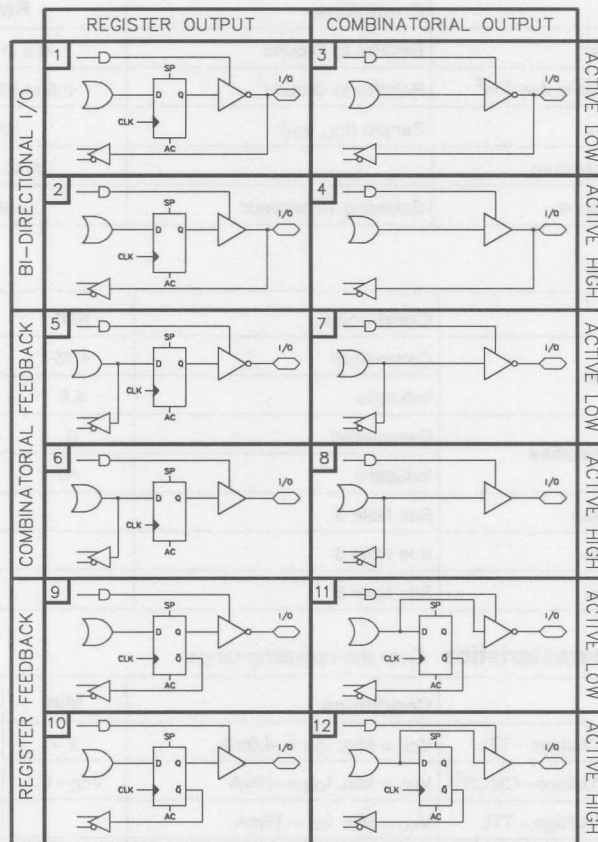


Figure 5. Equivalent Circuits for the Twelve Configurations of the PEEL20CG10A I/O Macrocell.

#	Configuration				Input/Feedback Select	Output Select	
	A	B	C	D			
1	0	0	1	0	Bi-Directional I/O	Register	Active Low
2	1	0	1	0	"	"	Active High
3	0	1	0	0	"	Combinatorial	Active Low
4	1	1	0	0	"	"	Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1	"	"	Active High
7	0	1	1	1	"	Combinatorial	Active Low
8	1	1	1	1	"	"	Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0	"	"	Active High
11	0	1	1	0	"	Combinatorial	Active Low
12	1	1	1	0	"	"	Active High

Table 1. PEEL20CG10A Macrocell Configuration Bits

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T _A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T _R	Clock Rise Time	See Note 3		20	ns
T _F	Clock Fall Time	See Note 3		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 3		250	ms

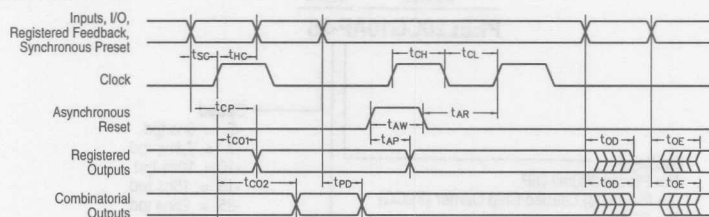
D.C. Electrical Characteristics Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage - CMOS ¹³	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{OLc}	Output LOW Voltage - CMOS ¹³	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		-0.3	0.8	V
I _{IL}	Input and I/O Leakage Current	V _{CC} = Max, GND ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V _O ≤ V _{CC}		±10	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5V, V _O = 0.5V ⁹ , T _A = 25°C	-30	-135	mA
I _{CC} ¹⁰	V _{CC} Current, f=1MHz	V _{IN} = 0V or 3V All outputs disabled ⁴	-5	140	mA
			-7	155	
			-10/I-10	135/145	
			-15/I-15	135/145	
			L-15	75	
			-25/I-25	67/75	
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT} ⁷	Output Capacitance			12	pF

A.C. Electrical Characteristics

 Over the Operating Range ^{8, 11}

Symbol	Parameter	-5		-7		-10 / I-10		-15 / I-15		L-15		-25 / I-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD}	Input ⁵ to non-registered output		5		7.5		10		15		15		25	ns
t _{OE}	Input ⁵ to output enable ⁶		5		7.5		10		15		15		25	ns
t _{OD}	Input ⁵ to output disable ⁶		5		7.5		10		15		15		25	ns
t _{CO1}	Clock to output		4		5.5		6		8		10		15	ns
t _{CO2}	Clock to comb. output delay via int. registered feedback		7.5		10		12		17		19		35	ns
t _{CF}	Clock to Feedback		2.5		3.5		4		5		6		9	ns
t _{SC}	Input ⁵ or feedback setup to clk	3		3		4/5		8		10		15		ns
t _{HC}	Input ⁵ hold after clock	0		0		0		0		0		0		ns
t _{CL} , t _{CH}	Clk low time, clock high time ⁸	2.5		3		5		6		7.5		13		ns
t _{CP}	Min Clk period Ext (t _{SC} + t _{CO1})	7		8.5		11		18		20		30		ns
f _{MAX1}	Int. Feedback (1/t _{SC} +t _{CF}) ¹²	181.8		142		111		76.9		62.5		41.6		MHz
f _{MAX2}	External Feedback (1/t _{CP}) ¹²	142.8		117		90.9		62.5		50		33.3		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹²	200		166		125		83.3		66.7		38.4		MHz
t _{AW}	Asynch. Reset pulse width	5		7.5		10		15		15		25		ns
t _{AP}	Input ⁵ to Asynchronous Reset		5		7.5		10		15		18		25	ns
t _{AR}	Asynch. Reset recovery time		5		7.5		10		15		18		25	ns
t _{RESET}	Power-on reset time for registers in clear state		5		5		5		5		5		5	μs

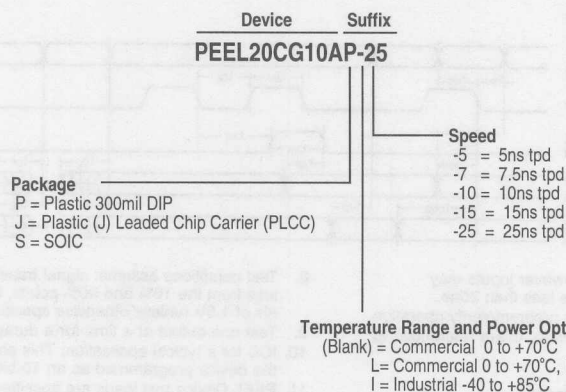
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Switching Waveforms

Notes

- Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
- V_I and V_O are not specified for program/verify operation.
- Test points for Clock and V_{CC} in t_r, t_f are referenced at 10% and 90% levels.
- I/O pins are 0V or V_{CC}.
- "Input" refers to an Input pin signal.
- t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; V_{REF} = V_L see test loads in Section 6 of this Data Book.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- Test one output at a time for a duration of less than 1 sec.
- ICC for a typical application: This parameter is tested with the device programmed as an 10-bit Counter.
- PEEL Device test loads are specified in Section 6 of this Data Book.
- Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
- Available only for 20CG10A-15/I-15/L-15/25/I-25 grades.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL20CG10AJ-5	5ns	C	J28
PEEL20CG10AP-7	7.5ns	C	P24
PEEL20CG10API-7	7.5ns	I	P24
PEEL20CG10AJ-7	7.5ns	C	J28
PEEL20CG10AJI-7	7.5ns	I	J28
PEEL20CG10AS-7	7.5ns	C	S24
PEEL20CG10ASI-7	7.5ns	I	S24
PEEL20CG10AP-10	10ns	C	P24
PEEL20CG10API-10		I	P24
PEEL20CG10AJ-10	10ns	C	J28
PEEL20CG10AJI-10		I	J28
PEEL20CG10AS-10	10ns	C	S24
PEEL20CG10ASI-10		I	S24
PEEL20CG10AP-15	15ns	C	P24
PEEL20CG10API-15		I	P24
PEEL20CG10AJ-15	15ns	C	J28
PEEL20CG10AJI-15		I	J28
PEEL20CG10AS-15	15ns	C	S24
PEEL20CG10ASI-15		I	S24
PEEL20CG10APL-15	15ns	C	P24
PEEL20CG10AJL-15	15ns	C	J28
PEEL20CG10ASL-15	15ns	C	S24
PEEL20CG10AP-25	25ns	C	P24
PEEL20CG10API-25		I	P24
PEEL20CG10AJ-25	25ns	C	J28
PEEL20CG10AJI-25		I	J28
PEEL20CG10AS-25	25ns	C	S24
PEEL20CG10ASI-25		I	S24

Part Number



PEEL™ 22CV10A -5/-7/-10/-15/L-15/-25 CMOS Programmable Electrically Erasable Logic

Features

- **High Speed/Low Power**
 - Speeds ranging from 5ns to 25ns
 - Power as low as 67mA at 25MHz
- **Electrically Erasable Technology**
 - Superior factory testing
 - Reprogrammable in plastic package
 - Reduces retrofit and development costs
- **Development/Programmer Support**
 - Third party software and programmers
 - ICT PLACE Development Software and PDS-3 programmer
- **Architectural Flexibility**
 - 132 product term X 44 input AND array
 - Up to 22 inputs and 10 outputs
 - Up to 12 configurations per macrocell
 - Synchronous preset, asynchronous clear
 - Independent output enables
 - 24-pin DIP/SOIC/TSSOP and 28-pin PLCC
- **Application Versatility**
 - Replaces random logic
 - Pin and JEDEC compatible with 22V10
 - Enhanced Architecture fits more logic than ordinary PLDs

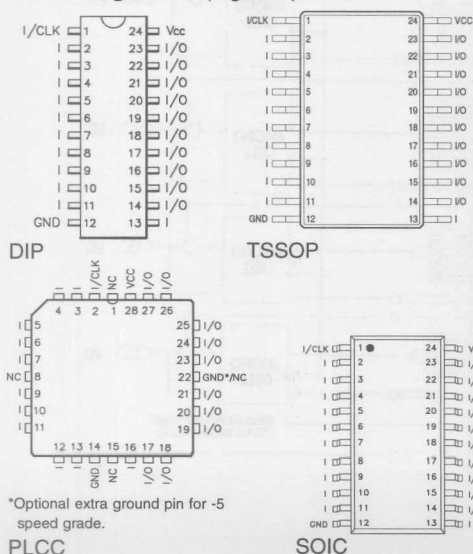
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General Description

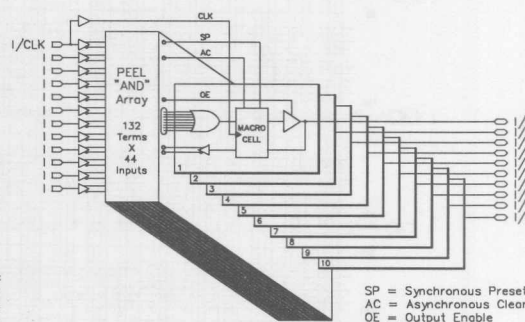
The PEEL22CV10A is a Programmable Electrically Erasable Logic (PEEL) device providing an attractive alternative to ordinary PLDs. The PEEL22CV10A offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL22CV10A is available in 24-pin DIP, SOIC, TSSOP and 28-pin PLCC packages with speeds ranging from 5ns to 25ns with power consumption as low as 67mA. EE-Reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Reprogrammability also improves factory testability, thus ensuring the highest quality possible. The PEEL22CV10A is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e., 22CV10A+). The additional macrocell configurations allow more logic to be put into every design. Development and programming support for the PEEL22CV10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

mability also improves factory testability, thus ensuring the highest quality possible. The PEEL22CV10A is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e., 22CV10A+). The additional macrocell configurations allow more logic to be put into every design. Development and programming support for the PEEL22CV10A is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



Block Diagram (Figure 2)



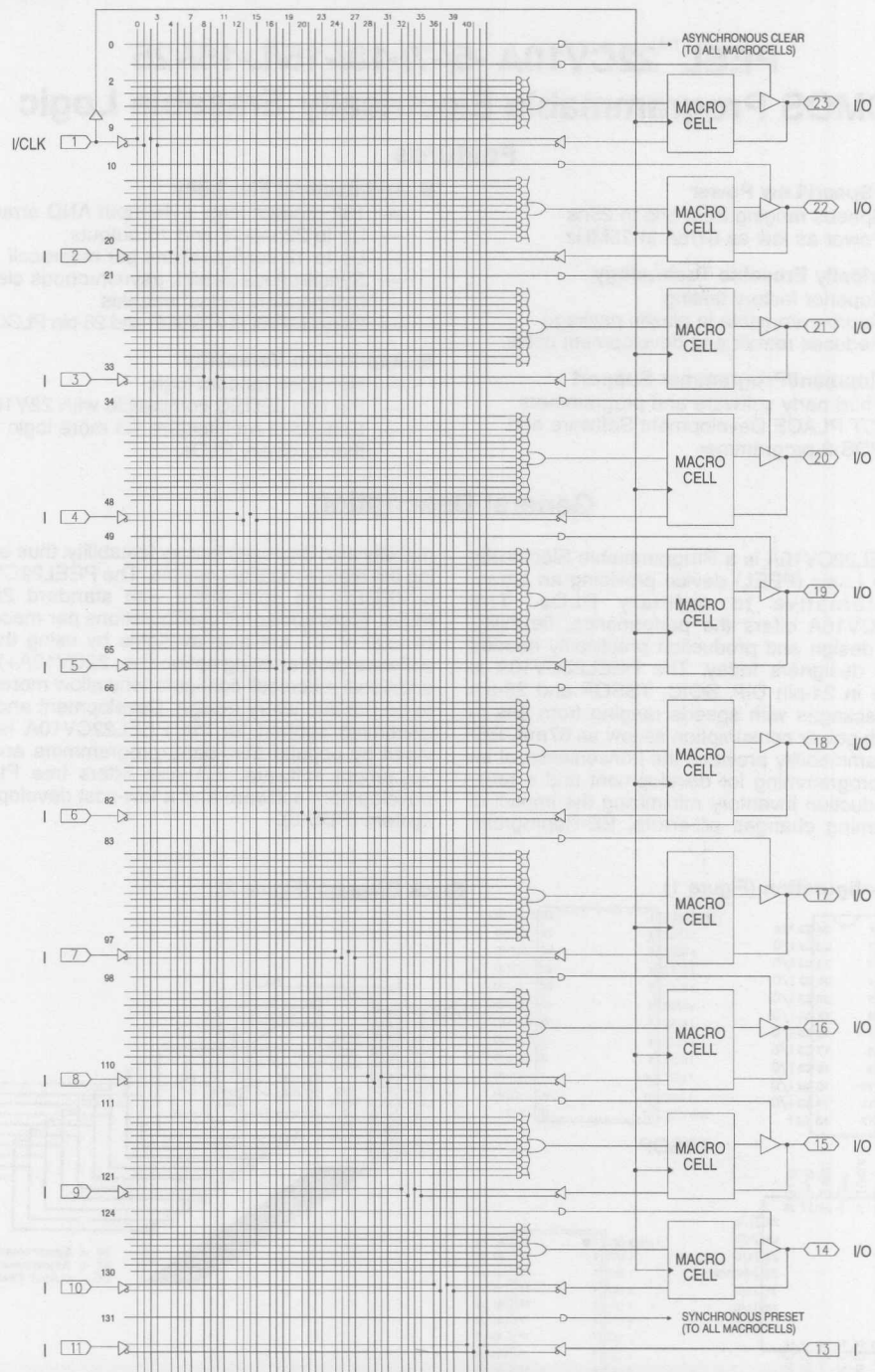


Figure 3. PEEL22CV10A Logic Array Diagram

Function Description

The PEEL22CV10A implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL22CV10A architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL22CV10A can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active-high or active-low polarity.

AND/OR Logic Array

The programmable AND array of the PEEL22CV10A (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14 and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous present term
- 1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE, and thus will not effect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE.

When programming the PEEL22CV10A, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND ar-

ray. (Note that PEEL device programmers automatically program the connections on unused product terms so that they will have no effect on the output function.)

Variable Product Term Distribution

The PEEL22CV10A provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Figure 3). This distribution allows optimum use of device resources.

Programmable I/O Macrocell

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL22CV10A to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the two EEPROM bits controlling these multiplexers (refer to Table 1). These bits determine output polarity and output type (registered or non-registered). Equivalent circuits for the four macrocell configurations are illustrated in Figure 5.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently

enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5), the Q output of the flip-flop drives the feedback term. When configuring an I/O macrocell to implement a combinatorial function (configurations 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directional I/O. (Refer also to Table 1.)

Additional Macro Cell Configurations

Besides the standard four-configuration macrocell shown in Figure 5, each PEEL22CV10A provides an additional eight configurations that can be used to increase design flexibility. The configurations are the same provided by the PEEL18CV8 and PEEL22CV10AZ. However, to maintain JEDEC file compatibility with standard 22V10 PLDs the additional configurations can only be utilized by speci-

fying the PEEL22CV10A+ for logic assembly and programming. To reference these additional configurations please refer to the PEEL22CV10A+ specifications at the end of this data sheet.

Design Security

The PEEL22CV10A provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step after the device has been programmed. Once the security bit is set, it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 24-bit code to be programmed into the PEEL22CV10A if the PEEL22CV10A+ software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

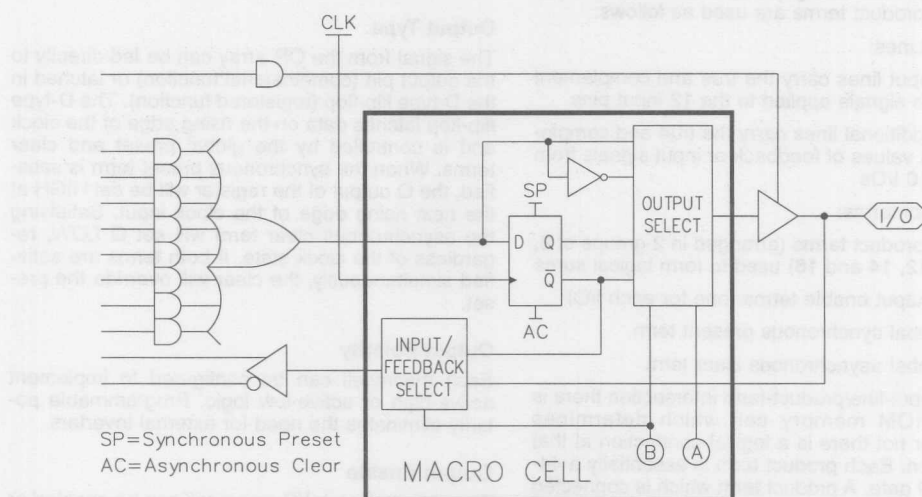
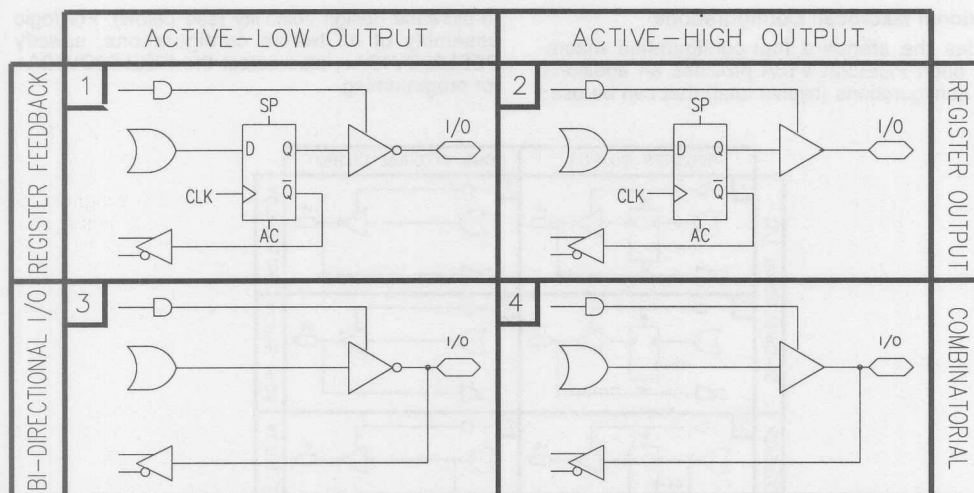


Figure 4. Block Diagram of the PEEL22CV10A I/O Macrocell



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Figure 5. Equivalent Circuits for the Four Configurations of the PEEL22CV10A I/O Macrocell.

Configuration			Input/Feedback Select	Output Select	
#	A	B			
1	0	0	Register Feedback	Register	Active Low
2	1	0			Active High
3	0	1	Bi-Directional I/O	Combinatorial	Active Low
4	1	1			Active High

Table 1. PEEL22CV10A Macrocell Configuration Bits

Additional Macrocell Configurations

Besides the standard four-configuration macrocells, each PEEL22CV10A provides an additional eight configurations (twelve total) that can be used

to increase design flexibility (see below). For logic assembly of all twelve configurations, specify PEEL22CV10A+, also select the PEEL22CV10A+ for programming.

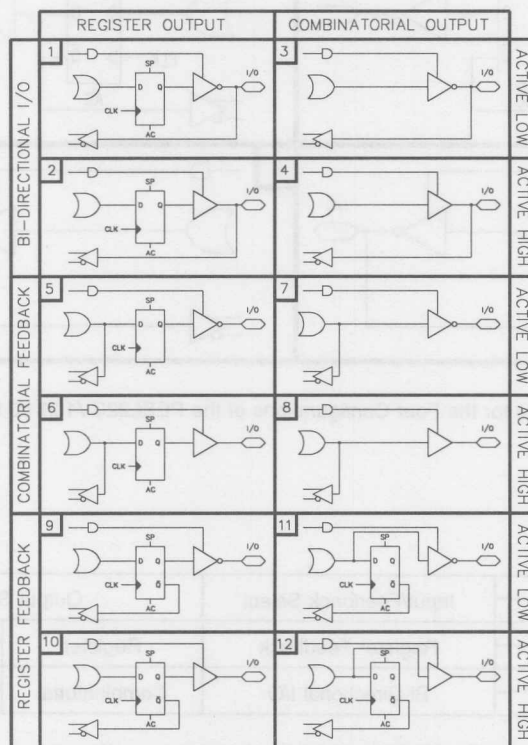


Figure 6. Equivalent Circuits for the Twelve Configurations of the PEEL22CV10A+ I/O Macrocell.

Configuration					Input/Feedback Select		Output Select	
#	A	B	C	D				
1	0	0	1	0	Bi-Directional I/O		Register	Active Low
2	1	0	1	0	"		"	Active High
3	0	1	0	0	"		Combinatorial	Active Low
4	1	1	0	0	"		"	Active High
5	0	0	1	1	Combinatorial Feedback		Register	Active Low
6	1	0	1	1	"		"	Active High
7	0	1	1	1	"		Combinatorial	Active Low
8	1	1	1	1	"		"	Active High
9	0	0	0	0	Register Feedback		Register	Active Low
10	1	0	0	0	"		"	Active High
11	0	1	1	0	"		Combinatorial	Active Low
12	1	1	1	0	"		"	Active High

Table 2. PEEL22CV10A+ Macrocell Configuration Bits

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

3

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T _A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T _R	Clock Rise Time	See Note 3		20	ns
T _F	Clock Fall Time	See Note 3		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 3		250	ms

D.C. Electrical Characteristics Over the operating range

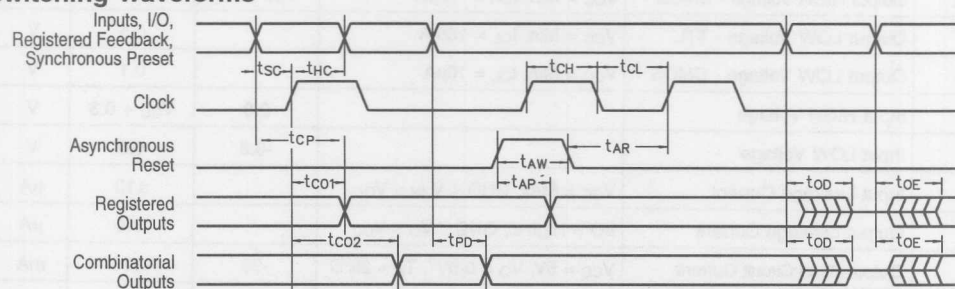
Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage - CMOS ¹³	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{OLc}	Output LOW Voltage - CMOS ¹³	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
I _{IL}	Input Leakage Current	V _{CC} = Max, GND ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V _O ≤ V _{CC}		±10	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5V, V _O = 0.5V ⁹ , T _A = 25°C	-30	-135	mA
I _{CC} ¹⁰	V _{CC} Current (See CR-1 for typical I _{CC})	V _{IN} = 0V or 3V f = 25MHz All outputs disabled ⁴	-5	140	mA
			-7	155	
			-10/I-10	135/145	
			-15/I-15	135/145	
			L-15	75	
			-25/I-25	67/75	
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT} ⁷	Output Capacitance			12	pF

A.C. Electrical Characteristics

Over the Operating Range ^{8, 11}

Symbol	Parameter	-5		-7		-10 / I-10		-15 / I-15		L-15		-25 / I-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD}	Input ⁵ to non-registered output		5		7.5		10		15		15		25	ns
t _{OE}	Input ⁵ to output enable ⁶		5		7.5		10		15		15		25	ns
t _{OD}	Input ⁵ to output disable ⁶		5		7.5		10		15		15		25	ns
t _{CO1}	Clock to output		4		5.5		6		8		10		15	ns
t _{CO2}	Clock to comb. output delay via internal registered feedback		7.5		10		12		17		19		35	ns
t _{CF}	Clock to Feedback		2.5		3.5		4		5		6		9	ns
t _{SC}	Input ⁵ or feedback setup to clock	3		3		5		8		10		15		ns
t _{HC}	Input ⁵ hold after clock	0		0		0		0		0		0		ns
t _{CL} , t _{CH}	Clock low time, clock high time ⁸	2.5		3		4		6		7.5		13		ns
t _{CP}	Min clock period Ext (t _{SC} + t _{CO1})	7		8.5		11		18		20		30		ns
f _{MAX1}	Internal Feedback (1/t _{SC} +t _{CF}) ¹²	181.6		142		111		76.9		62.5		41.6		MHz
f _{MAX2}	External Feedback (1/t _{CP}) ¹²	142.8		117		90.9		62.5		50		33.3		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹²	200		166		125		83.3		66.7		38.4		MHz
t _{AW}	Asynchronous Reset pulse width	5		7.5		10		15		15		25		ns
t _{AP}	Input ⁵ to Asynchronous Reset	5		7.5		10		15		18		25		ns
t _{AR}	Asynch. Reset recovery time	5		7.5		10		15		18		25		ns
t _{RESET}	Power-on reset time for registers in clear state	5		5		5		5		5		5		μs

Switching Waveforms



Notes

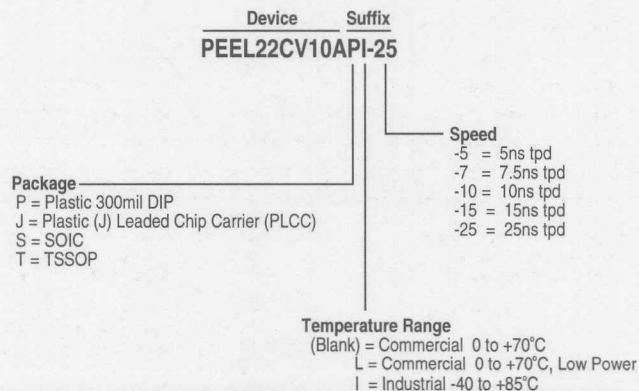
- Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
- V_I and V_O are not specified for program/verify operation.
- Test points for Clock and V_{CC} in t_r, t_f are referenced at 10% and 90% levels.
- I/O pins are 0V and 3V.
- "Input" refers to an Input pin signal.
- t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; V_{REF} = V_L see test loads in Section 6 of this Data Book.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- Test one output at a time for a duration of less than 1 sec.
- ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
- PEEL Device test loads are specified in Section 6 of this Data Book.
- Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
- Available only for 22CV10A -15/I-15/L-15/25/I-25 grades.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL22CV10AJ-5	5ns	C	J28
PEEL22CV10AP-7	7.5ns	C	P24
PEEL22CV10API-7	7.5ns	I	P24
PEEL22CV10AJ-7	7.5ns	C	J28
PEEL22CV10AJI-7	7.5ns	I	J28
PEEL22CV10AS-7	7.5ns	C	S24
PEEL22CV10ASI-7	7.5ns	I	S24
PEEL22CV10AP-10	10ns	C	P24
PEEL22CV10API-10	10ns	I	P24
PEEL22CV10AJ-10	10ns	C	J28
PEEL22CV10AJI-10	10ns	I	J28
PEEL22CV10AS-10	10ns	C	S24
PEEL22CV10ASI-10	10ns	I	S24
PEEL22CV10AP-15	15ns	C	P24
PEEL22CV10API-15	15ns	I	P24
PEEL22CV10AJ-15	15ns	C	J28
PEEL22CV10AJI-15	15ns	I	J28
PEEL22CV10AS-15	15ns	C	S24
PEEL22CV10ASI-15	15ns	I	S24
PEEL22CV10APL-15	15ns	C	P24
PEEL22CV10AJL-15	15ns	C	J28
PEEL22CV10ASL-15	15ns	C	S24
PEEL22CV10AP-25	25ns	C	P24
PEEL22CV10API-25	25ns	I	P24
PEEL22CV10AJ-25	25ns	C	J28
PEEL22CV10AJI-25	25ns	I	J28
PEEL22CV10AS-25	25ns	C	S24
PEEL22CV10ASI-25	25ns	I	S24

Contact ICT for availability of this device in TSSOP packages.

Part Number



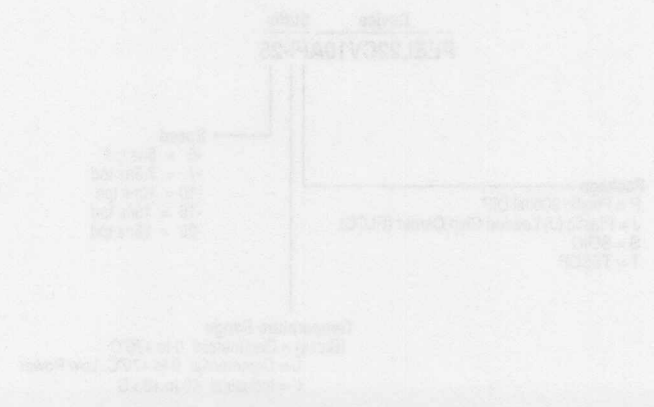


Ordering Information

Part Number	Quantity	Weight (lb)	Dimensions (in)
PEEL-220V10A-1	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-2	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-3	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-4	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-5	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-6	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-7	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-8	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-9	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-10	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-11	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-12	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-13	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-14	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-15	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-16	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-17	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-18	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-19	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-20	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-21	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-22	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-23	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-24	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-25	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-26	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-27	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-28	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-29	100	10.0	10.0 x 10.0 x 1.0
PEEL-220V10A-30	100	10.0	10.0 x 10.0 x 1.0

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Part Number



PEELTM 22CV10AZ -15/-25 CMOS Programmable Electrically Erasable Logic Device

Features

■ Ultra Low Power

- $I_{CC} = 25\mu A$ (typical) at standby
- $I_{CC} = 3.5mA$ (typical) at 1MHz
- $t_{PD} = 15ns$ and $25ns$ versions

■ CMOS Electrically Erasable Technology

- Superior factory testing
- Reprogrammable in plastic package
- Reduces retrofit and development costs

■ Development/Programmer Support

- Third party software and programmers
- ICT PLACE Development Software and PDS-3 programmer

■ Architectural Flexibility

- 133 product term x 44 input AND array
- Up to 22 inputs and 10 I/O pins
- 12 possible macrocell configurations
- Synchronous preset, asynchronous clear
- Independent output enables
- Programmable clock source and polarity
- 24-pin DIP/SOIC/TSSOP and 28-pin PLCC

■ Application Versatility

- Replaces random logic
- Pin and JEDEC compatible with 22V10
- Ideal for power-sensitive systems
- Enhanced architecture options

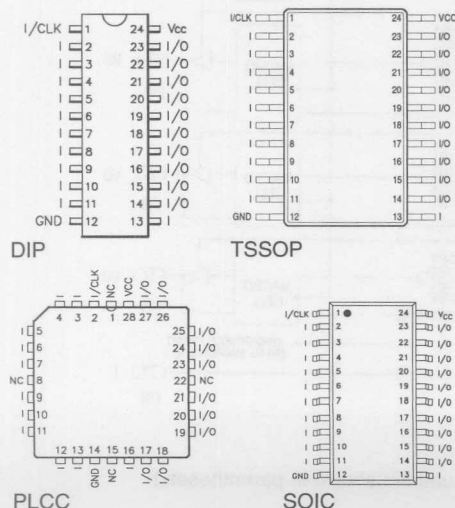
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General Description

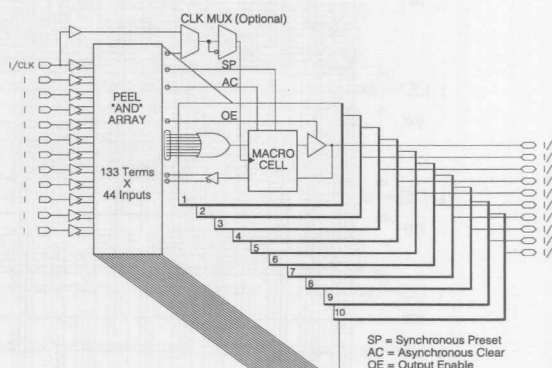
The PEEL22CV10AZ is a Programmable Electrically Erasable Logic (PEEL) device that provides a low power alternative to ordinary PLDs. The PEEL22CV10AZ is available in 24-pin DIP, SOIC, TSSOP and 28-pin PLCC packages. A "zero-power" ($100\mu A$ max. I_{CC}) standby mode makes the PEEL22CV10AZ ideal for power sensitive applications such as handheld meters, portable communication equipment and laptop computers/peripherals. EE-reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-Re-programmability also improves factory testability,

thus ensuring the highest quality possible. The PEEL22CV10AZ is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e. 22CV10AZ+). The additional macrocell configurations allow more logic to be put into every device, potentially reducing the design's component count and lowering the power requirements even further. Development and programming support for the PEEL22CV10AZ is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



Block Diagram (Figure 2)



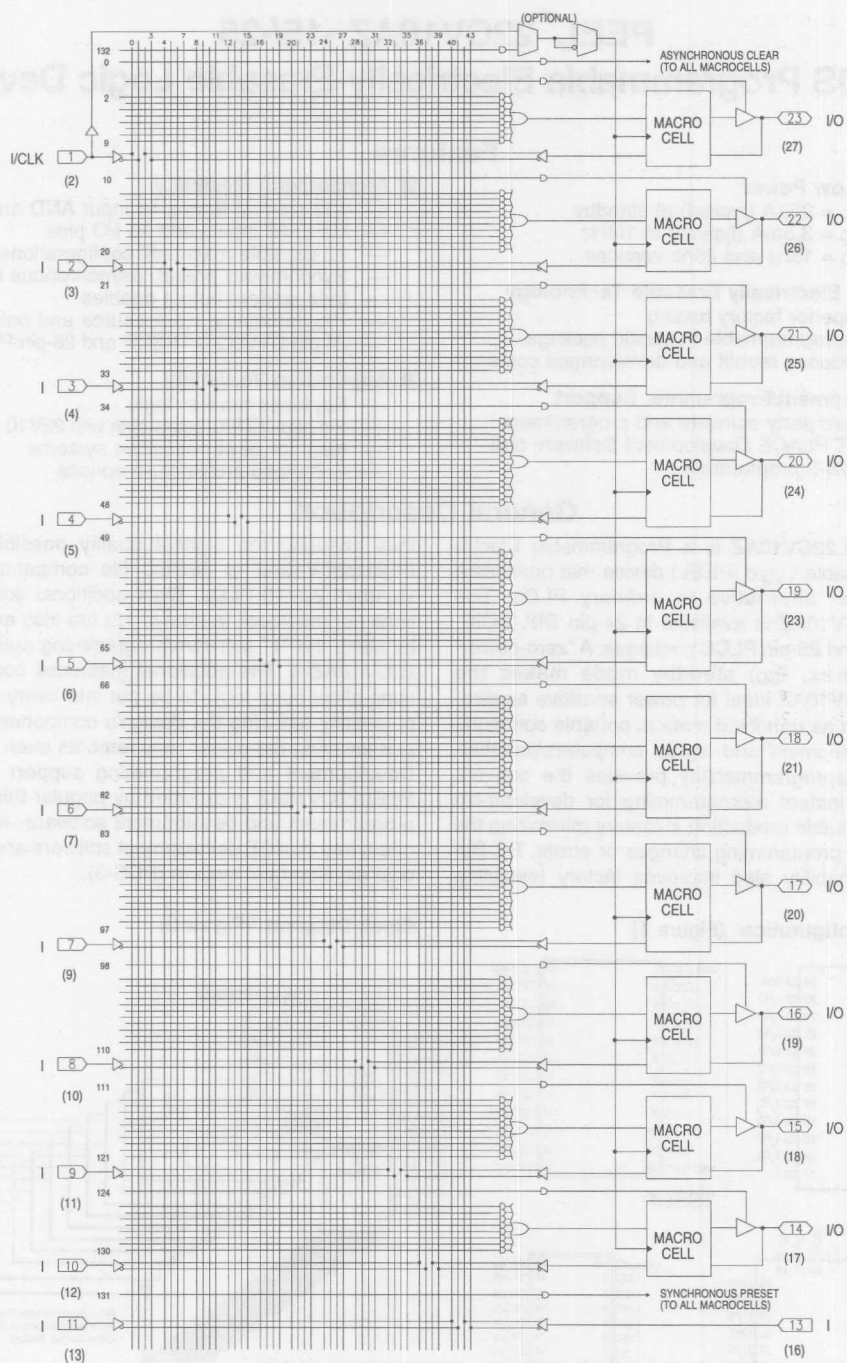


Figure 3. PEEL22CV10AZ Logic Array Diagram
(Pin numbers are for DIP and SOIC packages, PLCC pin numbers shown in parentheses.)

Function Description

The PEEL22CV10AZ implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL22CV10AZ architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and ten I/Os provide up to 22 inputs and 10 outputs for creating logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL22CV10AZ can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations in standard 22V10 mode, or any one of 12 configurations using the special "plus" mode.

The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array. See the PEEL22CV10A data sheet for macrocell architectural details.

Programmable Clock Options

A unique feature of the PEEL22CV10AZ is a programmable clock multiplexer which allows the user to select true or complement forms of either pin or product-term clock sources.

Zero Power Feature

The CMOS PEEL22CV10AZ features "Zero-Power" standby operation for ultra-low power consumption. With the "Zero-Power" feature, transition-detection circuitry monitors the inputs, I/Os (including CLK) and feedbacks. If these signals do not change for a period of time equal to approximately $[t_{PD}]$, the outputs are latched in their current state and the device automatically powers down. When the next signal transition is detected, the device will "wake up" for active operation until the signals stop switching long enough to trigger the next power-down.

As a result of the "Zero Power" feature, significant power savings can be realized for combinatorial or sequential operations when the inputs or clock change at a modest rate. See Figure 4.

Design Security

The PEEL22CV10AZ provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL22CV10AZ if the PEEL22CV10AZ+ software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

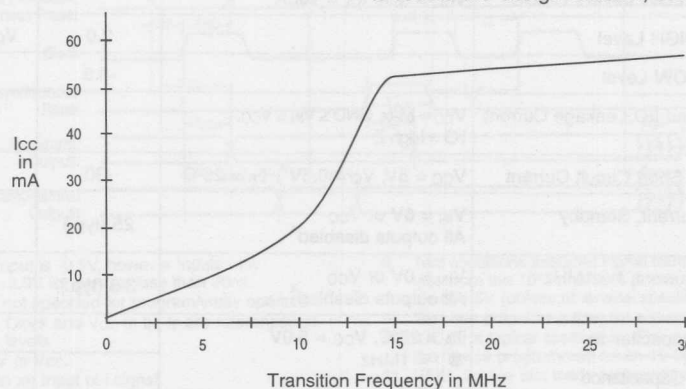


Figure 4. Typical I_{cc} vs Input or Clock transition frequency for 22CV10AZ

specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V _I , V _O	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
T _A	Ambient Temperature	Commercial	0	+70	°C
T _R	Clock Rise Time	See Note 3		20	ns
T _F	Clock Fall Time	See Note 3		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 3		250	ms

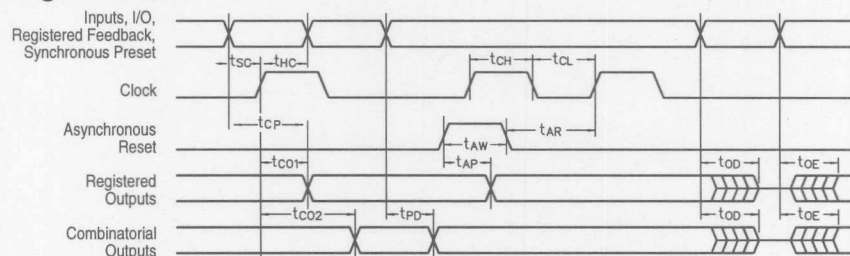
D.C. Electrical Characteristics Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHC}	Output HIGH Voltage - CMOS	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Level - TTL	V _{CC} = Min, I _{OL} = 16mA		0.5	V
V _{OLC}	Output LOW Level - CMOS	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		-0.3	0.8	V
I _{IL}	Input and I/O Leakage Current	V _{CC} = Max, GND ≤ V _{IN} ≤ V _{CC} , I/O = High Z		±10	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5V, V _O = 0.5V ⁹ , T _A = 25°C	-30	-135	mA
I _{CCS}	V _{CC} Current, Standby	V _{IN} = 0V or V _{CC} All outputs disabled ⁴	25 (typ.)	100	μA
I _{CC} ¹⁰	V _{CC} Current, f = 1MHz	V _{IN} = 0V or V _{CC} All outputs disabled ⁴	3.5 (typ.)	5	mA
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT} ⁷	Output Capacitance			12	pF

A.C. Electrical Characteristics

 Over the Operating Range ^{8, 11}

Symbol	Parameter	-15		-25		Unit
		Min	Max	Min	Max	
t _{PD}	Input ⁵ to non-registered output		15		25	ns
t _{OE}	Input ⁵ to output enable ⁶		15		25	ns
t _{OD}	Input ⁵ to output disable ⁶		15		25	ns
t _{CO1}	Clock to output		10		15	ns
t _{CO2}	Clock to comb. output delay via internal registered feedback		19		35	ns
t _{CF}	Clock to Feedback		6		9	ns
t _{SC}	Input ⁵ or feedback setup to clock	10		15		ns
t _{HC}	Input ⁵ hold after clock	0		0		ns
t _{CL} , t _{CH}	Clock low time, clock high time ⁸	7.5		13		ns
t _{CP}	Min clock period Ext (t _{SC} + t _{CO1})	20		30		ns
f _{MAX1}	Internal Feedback (1/t _{SC} +t _{CF}) ¹²	62.5		41.6		MHz
f _{MAX2}	External Feedback (1/t _{CP}) ¹²	50		33.3		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹²	66.7		38.4		MHz
t _{AW}	Asynchronous Reset pulse width	15		25		ns
t _{AP}	Input ⁵ to Asynchronous Reset		18		25	ns
t _{AR}	Asynchronous Reset recovery time		18		25	ns
t _{RESET}	Power-on reset time for registers in clear state		5		5	μs

Switching Waveforms

Notes

- Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
- V_I and V_O are not specified for program/verify operation.
- Test points for Clock and V_{CC} in t_r, t_f are referenced at 10% and 90% levels.
- I/O pins are 0V or V_{CC}.
- "Input" refers to an Input pin signal.
- t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; V_{REF} = V_L see test loads in Section 6 of this Data Book.
- Capacitances are tested on a sample basis.

- Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- Test one output at a time for a duration of less than 1 sec.
- ICC for a typical application: This parameter is tested with the device programmed as an 10-bit Counter.
- PEEL Device test loads are specified in Section 6 of this Data Book.
- Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL22CV10AZP-15	15ns	C	P24
PEEL22CV10AZJ-15	15ns	C	J28
PEEL22CV10AZS-15	15ns	C	S24
PEEL22CV10AZP-25	25ns	C	P24
PEEL22CV10AZJ-25	25ns	C	J28
PEEL22CV10AZS-25	25ns	C	S24

Contact ICT for availability of this device in TSSOP packages.

Part Number

Device Suffix
PEEL22CV10AZP-25

Package

P = Plastic 300mil DIP
J = Plastic (J) Leaded Chip Carrier (PLCC)
S = SOIC
T = TSSOP

Speed

-15 = 15ns tpd
-25 = 25ns tpd

Temperature Range

(Blank) = Commercial 0 to +70°C

PEEL™ 22LV10AZ -25 **CMOS Programmable Electrically Erasable Logic Device**

Features

- **Low Voltage, Ultra Low Power Operation**
 - $V_{CC} = 2.7$ to $3.6V$
 - $I_{CC} = 25\mu A$ (typical) at standby
 - $I_{CC} = 2mA$ (typical) at 1MHz
- **CMOS Electrically Erasable Technology**
 - Superior factory testing
 - Reprogrammable in plastic package
 - Reduces retrofit and development costs
- **Development/Programmer Support**
 - Third party software and programmers
 - ICT PLACE Development Software and PDS-3 programmer

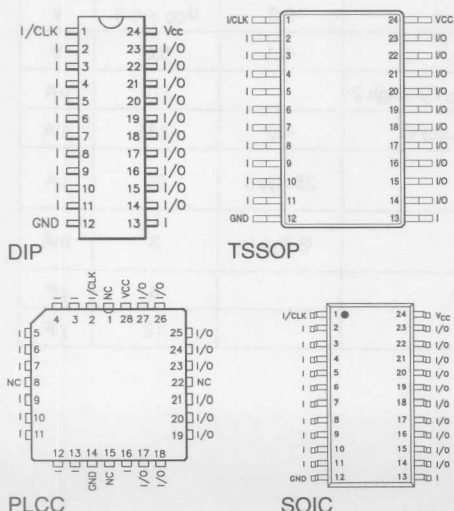
- **Architectural Flexibility**
 - 133 product term x 44 input AND array
 - Up to 22 inputs and 10 I/O pins
 - 12 possible macrocell configurations
 - Synchronous preset, asynchronous clear
 - Independent output enables
 - Programmable clock source and polarity
 - 24-pin DIP/SOIC/TSSOP and 28-pin PLCC
- **Application Versatility**
 - Replaces random logic
 - Pin and JEDEC compatible with 22V10
 - Ideal for power-sensitive systems
 - Enhanced architecture options

General Description

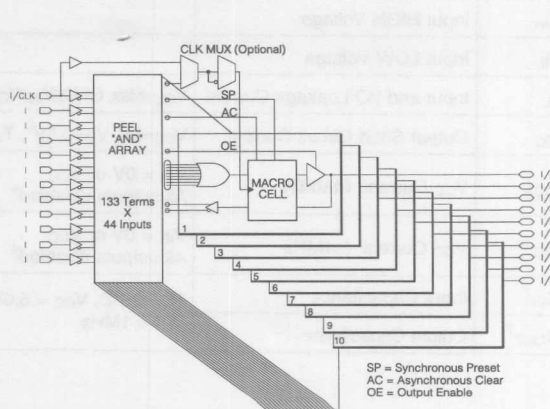
The PEEL22LV10AZ is a Programmable Electrically Erasable Logic (PEEL) device that provides a low voltage version of the PEEL22CV10AZ. The PEEL22LV10AZ is available in 24-pin DIP, SOIC, TSSOP and 28-pin PLCC packages (see Figure 1). A "zero-power" ($50\mu A$ max. I_{CC}) standby mode makes the PEEL22LV10AZ ideal for battery-powered or power-sensitive applications such as handheld meters, portable communication equipment and laptop computers/peripherals. EE-reprogrammability provides the convenience of instant reprogramming for development and a reusable production inventory minimizing the impact of programming changes or errors. EE-reprogrammability also improves factory testability, thus

ensuring the highest quality possible. The PEEL22LV10AZ is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e., 22LV10AZ+). In both the standard 22V10 and "plus" modes, the PEEL22LV10AZ has exactly the same architectural features as the 5 volt PEEL22CV10AZ. See Figure 2 and the PEEL22CV10AZ data sheet for details. Development and programming support for the PEEL22LV10AZ is provided by popular third-party programmers and development software. ICT also offers free PLACE development software and a low-cost development system (PDS-3).

Pin Configuration (Figure 1)



Block Diagram (Figure 2)



This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to Ground	-0.5 to + 5.0	V
V _I , V _O	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	2.7	3.6	V
T _A	Ambient Temperature	Commercial	0	+70	°C
T _R	Clock Rise Time	See Note 3		20	ns
T _F	Clock Fall Time	See Note 3		20	ns
T _{RVCC}	V _{CC} Rise Time	See Note 3		250	ms

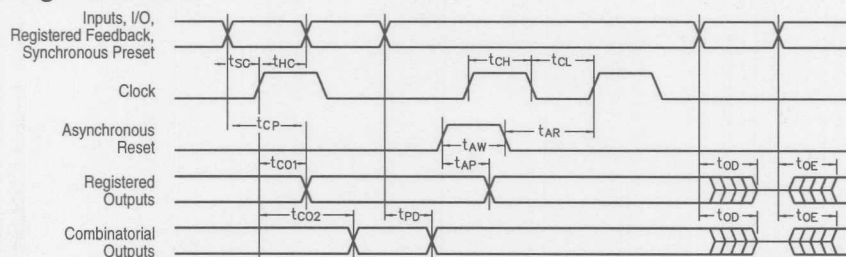
D.C. Electrical Characteristics Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} =Min, I _{OH} =-4.0mA	V _{CC} - 0.5		V
V _{OHc}	Output HIGH Voltage - CMOS	V _{CC} =Min, I _{OH} =-10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} =Min, I _{OL} =8mA		0.5	V
V _{OLc}	Output LOW Voltage - CMOS	V _{CC} =Min, I _{OL} =10μA		0.1	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.1	0.3	V
I _{IL}	Input and I/O Leakage Current	V _{CC} =Max, GND≤V _{IN} ≤V _{CC} , I/O=High Z		±10	μA
I _{SC}	Output Short Circuit Current	V _{CC} =5V, V _O =0.5V ⁹ , T _A =25°C	-30	-135	mA
I _{CCS}	V _{CC} Current, Standby	V _{IN} = 0V or V _{CC} All outputs disabled ⁴	25 (typ.)	50	μA
I _{CC} ¹⁰	V _{CC} Current, f=1MHz	V _{IN} = 0V or V _{CC} All outputs disabled ⁴	2 (typ.)	3	mA
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT} ⁷	Output Capacitance			12	pF

A.C. Electrical Characteristics

 Over the Operating Range ^{8, 11}

Symbol	Parameter	-25		Unit
		Min	Max	
t _{PD}	Input ⁵ to non-registered output		25	ns
t _{OE}	Input ⁵ to output enable ⁶		25	ns
t _{OD}	Input ⁵ to output disable ⁶		25	ns
t _{CO1}	Clock to output		15	ns
t _{CO2}	Clock to comb. output delay via internal registered feedback		35	ns
t _{CF}	Clock to Feedback		9	ns
t _{SC}	Input ⁵ or feedback setup to clock	15		ns
t _{HC}	Input ⁵ hold after clock	0		ns
t _{CL} , t _{CH}	Clock low time, clock high time ⁸	13		ns
t _{CP}	Min clock period Ext (t _{SC} + t _{CO1})	30		ns
f _{MAX1}	Internal Feedback (1/t _{SC} +t _{CF}) ¹²	41.6		MHz
f _{MAX2}	External Feedback (1/t _{CP}) ¹²	33.3		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹²	38.4		MHz
t _{AW}	Asynchronous Reset pulse width	25		ns
t _{AP}	Input ⁵ to Asynchronous Reset		25	ns
t _{AR}	Asynchronous Reset recovery time		25	ns
t _{RESET}	Power-on reset time for registers in clear state		5	μs

3
Switching Waveforms

Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_r, t_f are referenced at 10% and 90% levels.
4. I/O pins are 0V or V_{CC}.
5. "Input" refers to an Input pin signal.
6. t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH} - 0.1V or V_{OL} + 0.1V; V_{REF} = V_L see test loads in Section 6 of this Data Book.
7. Capacitances are tested on a sample basis.

8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration of less than 1 sec.
10. ICC for a typical application: This parameter is tested with the device programmed as an 10-bit Counter.
11. PEEL Device test loads are specified in Section 6 of this Data Book.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.

Ordering Information

PART NUMBER	SPEED	TEMPERATURE	PACKAGE
PEEL22LV10AZP-25	25ns	C	P24
PEEL22LV10AZJ-25	25ns	C	J28
PEEL22LV10AZS-25	25ns	C	S24

Contact ICT for availability of this device in TSSOP packages.

Part Number

Device Suffix
PEEL22LV10AZP-25

Speed
-25 = 25ns tpd

Package
P = Plastic 300mil DIP
J = Plastic (J) Leaded Chip Carrier (PLCC)
S = SOIC
T = TSSOP

Temperature Range
(Blank) = Commercial 0 to +70°C

Special Products and Services

MPA Mask-Programmed PEEL Arrays	4-3
Tape and Reel Specification	4-4

Special Products and Services

Mr. A Mach-Formed PEEL Arays	4-3
Tape and Peel Specification	4-4

MPA Mask-Programmed PEEL Arrays

Features

- **Reduced Cost for High-Volume Applications**
 - No NRE charges
 - 20% to 40% cost reduction, depending on volumes
- **Compatible with Programmable PEEL Arrays**
 - Pin and function compatible drop-in replacements for PA7024, PA7128, PA7140
 - Available in the same speed, temperature, and package options
- **Low Power**
 - 5 to 15mA typical current consumption
 - Reduce power by as much as 80% from programmable versions, especially at low frequencies
- **Easy Conversion between Programmable and Mask Versions**
 - Programmable PEEL Arrays for prototyping and early production
 - Mask-programmed PEEL Arrays for high-volume production
- **High Speed**
 - Speed grades from 15ns to 25ns
 - Match equivalent programmable PEEL Array speed grades
- **Simplified Manufacturing**
 - No programming necessary
 - No post-programming testing needed, all devices are factory tested

4

General Description

Mask-programmed PEEL Arrays (MPAs) are mask-programmed versions of ICT's popular Programmable Electrically Erasable Logic (PEEL) Arrays. MPAs provide a low-cost option for high volume production (greater than 5000 pieces) designs. As with reprogrammable PEEL Arrays, MPAs are available in 24- and 28-pin DIP and SOIC packages, as well as 28- and 44-pin PLCC packages. Speeds range from 15ns to 25ns, matching the speed grades available for the corresponding PEEL Arrays. MPAs provide all of the architectural benefits of PEEL Arrays (see the respective PEEL Array data sheets) with the lower costs and power consumption of mask-programmed components. With MPAs, component costs can be reduced by up to 40% and power consumption by up to 80%.

MPAs are pin and function compatible with the reprogrammable PEEL Arrays that they can replace. This compatibility allows easy transition from user-programmable components to mask-programmed versions for designs in production. See Figure 1. In addition, full forward and backwards compatibility ensures that designs which require revisions or enhancements can easily move back into programmable PEEL Arrays if necessary. Once the changes are complete and the design again reaches high volume production, a new MPA can be created. Together PEEL Arrays and MPAs provide the flexibility of programmable logic with the low cost and power consumption of masked components.

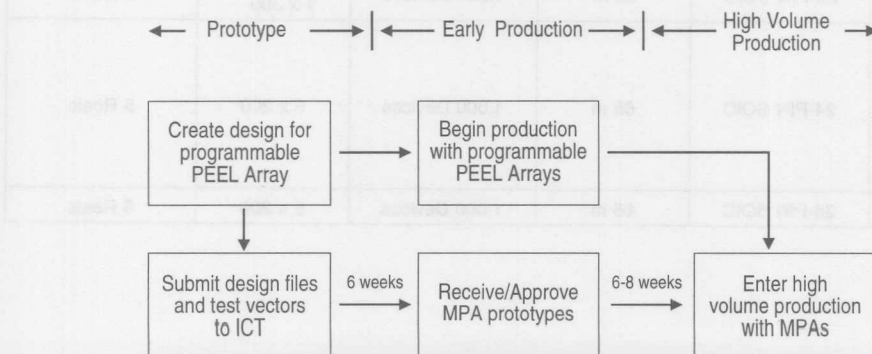


Figure 1. PEEL Array to MPA Design Flow

Tape-and-Reel Specification

General Description

ICT offers tape-and-reel packaging for our PLCC and SOIC products in order to provide a reliable storage and handling solution as well as to accommodate robotic handling/loading equipment. All ICT tape-and-reel containers are packaged in full compliance with the Electronics Industry Association Standard EIA-481-2.

Products requested to be packaged by tape-and-reel methods are placed individually in a pocketed plastic carrier tape. The devices are held in place by a protective tape that seals each device in its individual pocket. The loaded and sealed tape is then transferred to a plastic reel prior to storage and shipment.

Tape-and-reel packaging is available for all PLCC and SOIC package products from ICT. All orders for tape-and-reel product must clearly identify the special packaging request. Orders should be placed in the standard quantities listed below, unless otherwise approved by an ICT Area Sales Manager. Please contact your local ICT Manufacturer's Representative or Area Sales Manager for further information on tape-and-reel packaging.

Tape-and-Reel Ordering Information

Device	Package Type	Meters Per Reel	Standard QTY	QTY Per Reel	# of 13" Reels
16V8J 18CV8J	20-PIN PLCC	13.2 m	1,000 Devices	1 x 1000	1 Reel
20V8J 22CV8J 20CG10AJ 22CV10AJ 22CV10AZJ 22LV10AZJ 7024J 7128J	28-PIN PLCC	14 m	750 Devices	1 x 750	1 Reel
7140J	44-PIN PLCC	40 m	500 Devices	2 x 200 + 1 x 100	3 Reels
16V8S 18CV8S	20-PIN SOIC	65 m	1,000 Devices	2 x 350 + 1 x 300	3 Reels
20V8S 22CV8S 20CG10AS 22CV10AS 22CV10AZS 22LV10AZS 7024S	24-PIN SOIC	65 m	1,000 Devices	5 x 200	5 Reels
7128S	28-PIN SOIC	65 m	1,000 Devices	5 x 200	5 Reels

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PEEL Device and Array Smart Translator	5-6
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OrCAD-to-PEEL Advanced Device PDS-3 PEEL Development System Programming Support List

Development Tools

PLACE Advanced Development Software	B-3
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CURL-to-PEEL Advanced Device Filter	B-9
ORCAD-to-PEEL Advanced Device Filter	B-10
PD-3 PEEL Development System	B-11
Programming Support List	B-12

PLACETM Advanced Development Software for PEEL Arrays and PEEL Devices

Features

- **PEEL Architectural Compiler and Editor**
 - Advanced development support for PEEL Arrays and PEEL Devices
 - Runs on IBM compatible PCs
 - Fast and efficient design environment
- **Architectural Editing**
 - Graphic display and control of architecture
 - Equation and state machine entry
- **Logic Compilation**
 - Auto-transformation to sum-of-products
 - Five levels of logic reduction
- **Multi-level Logic Simulation**
 - Simulates internal and external signals
 - Interactive waveform editor and display
- **Translates Standard PLDs to PEEL Products**
 - Reads PLD (PAL, GAL, EPLD) JEDEC file then automatically translates to PEEL Devices and PEEL Arrays
- **Programmer Interface**
 - Interfaces to ICT's PDS and popular third party programmers

5

General Description

PLACE is an advanced development software package offering complete support for ICT's family of PEEL (Programmable Electrically Erasable Logic) Arrays and Devices. The innovative PLACE architectural editor enables graphical control of the device architecture, along with logic equation, truth table, and state machine entry, making the overall design process easy to understand. The PLACE compiler performs logic transformation so equations can be defined in a variety of formats. The compiler also features five levels of user-selectable logic reduction, including auto-demorganization,

making it possible to fit more logic into every design. PLACE also provides a multi-level logic simulator that lets the external and internal signals be fully simulated, analyzed and edited via a special waveform display. Documentation of PLACE designs is accomplished through batch printing of equations, architecture and waveform displays. System requirements for PLACE are: IBM PC compatible system with DOS version 3.0 or greater, 540K base memory, EGA or VGA graphics and mouse. PLACE also supports expanded memory systems with EMS drivers conforming to the 3.2 or greater LIM EMS specification.

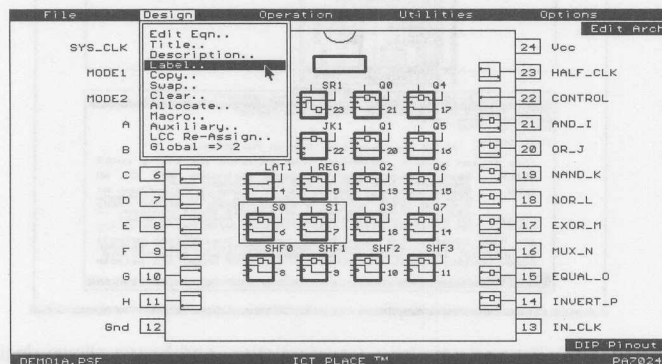


Figure 1. The PLACE architectural editor's "chip display" provides a global view of the design, allowing quick access to I/Os, registers, cells and equations.

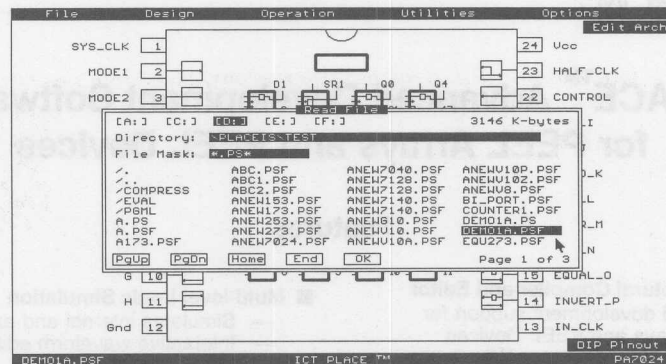


Figure 2. The PLACE software functions in a mouse-driven windows environment allowing easy access and control of all operations. Shown here is the file selection window.

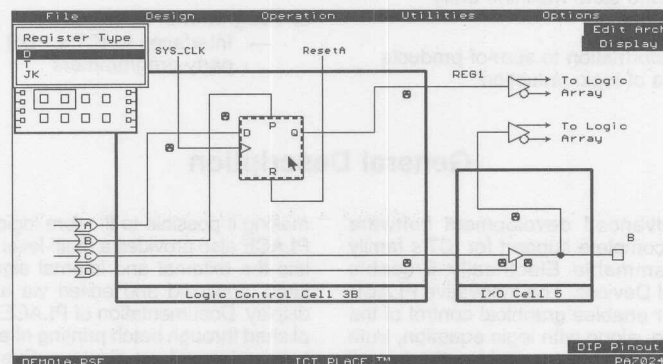


Figure 3. The architecture of each cell can be specified by selecting the desired architectural element with the mouse and then "clicking" through all possible configurations graphically on the screen. Shown here is the PA7024's register selection of D, T or JK flip-flops.

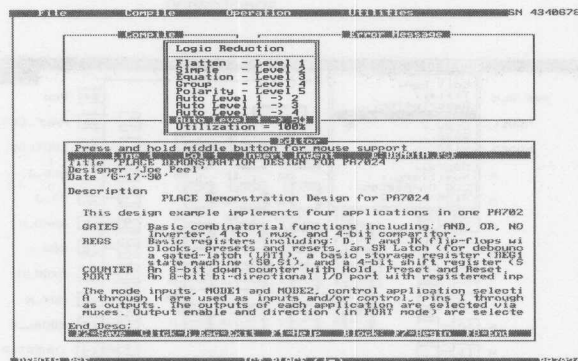


Figure 4. The PLACE compiler performs logic transformation, and hence allows designs to be specified in any fashion (i.e. equation, state-diagram or truth-table). The compiler also features five levels of user-selectable logic reduction, making it possible to fit more logic into every design.

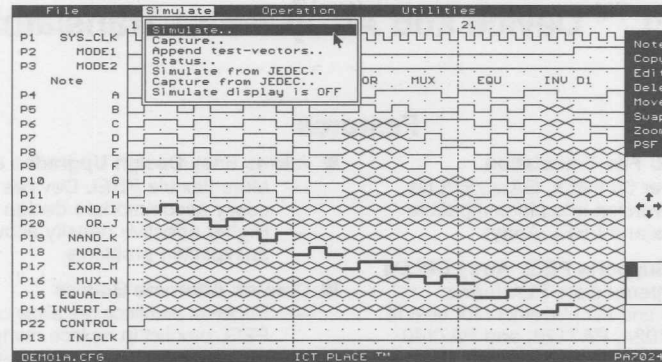


Figure 5. The PLACE logic simulator lets external and internal signals be fully simulated, analyzed and edited via a special waveform display. Output signals can be "captured" or simulated. Simulation errors are marked on the display for quick analysis.

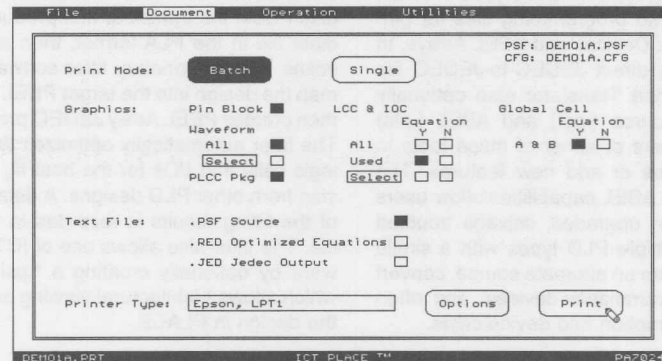


Figure 6. PLACE designs can be documented through batch or single printing of architectural configurations, waveform displays and logic descriptions including equations, state-diagrams and truth-tables.

PEEL™ Device and Array Smart Translator

Features

- **Automatic JEDEC File Translation**
 - Translates over 50 PALs, GALs, EPLDs
 - Supports conversion into pin-compatible PEEL Devices and PEEL Arrays
- **Advanced Fitter Supports PEEL Array CPLDs**
 - Works from intermediate PLA format
 - Optimizes cell and I/O placement for best fit
 - Supports PA7024, PA7128, and PA7140
- **Creates Optional PLACE Source File**
 - Enables design changes and additions
 - Allows architectural viewing of design
 - Provides JEDEC file waveform simulator
- **Allows Easy Design Upgrades and Fixes**
 - More flexible PEEL Devices and Arrays easily accommodate design upgrades
 - Higher effective density allows fixes for unexpected problems
- **Creates Alternate Source**
 - Superset architectures allow one type of PEEL product to replace many different PLDs
 - EE reprogrammability simplifies procurement and production and often reduces costs
- **System Requirements**
 - IBM-compatible PCs running DOS

General Description

The PEEL Smart Translator software tool allows designers to automatically convert JEDEC programming files from over 50 different types of PALs, GALs, and EPLDs into programming files for pin-compatible ICT PEEL Devices and PEEL Arrays. In addition to providing direct JEDEC-to-JEDEC file conversions, the Smart Translator also optionally produces PLACE source (.psf) and ABEL (.pla) files, which allow users of either of those tools to make design changes or add new features. The JEDEC, PLACE and ABEL capabilities allow users to make easy design upgrades, salvage troubled designs, replace multiple PLD types with a single type of ICT PLD, create an alternate source, convert to EEPROM reprogrammable devices, and often reduce power consumption and device costs.

For simple PLDs, such as 20/24-pin PALs, GALs and EPLDs, the PEEL Smart Translator performs a direct JEDEC-to-JEDEC translation. For more complex PLDs, the translator first produces an intermediate file in the PLA format, then automatically invokes ICT's proprietary fitter software to efficiently map the design into the target PEEL Array. The fitter then creates PEEL Array JEDEC programming files. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit, easing conversion from other PLD designs. A detailed description of the fitting results is recorded in the .rpt (report) file. The fitter also allows use of ICT's PLACE software by optionally creating a ".psf" extension file which allows architectural viewing and simulation of the design in PLACE.

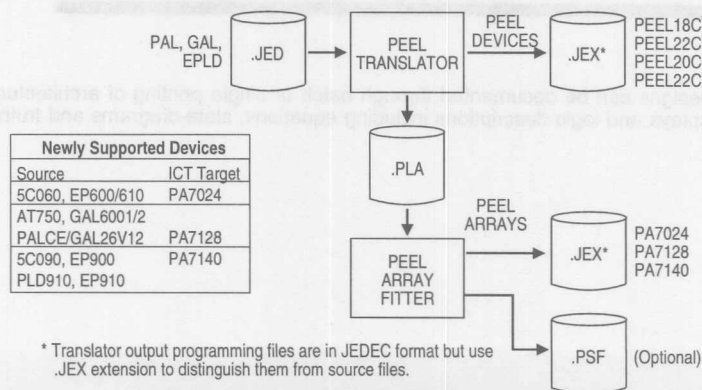


Figure 1. PEEL Translator Design Flow

ABEL-to-PEELTM (for DOS) Advanced Device Fitter

Features

- **PEEL Array Support for ABEL Software**
 - Supports PA7024, 7128 and 7140
 - Operates with ABEL 4.0 or greater
- **Maintains ABEL Design Methodology**
 - Design, compile, simulate with ABEL
 - Fitter creates JEDEC programming files
 - Operates on "Berkeley Espresso" PLA files
- **True Device Independent Design Entry**
 - I/O pin and node numbers need not be specified
 - Optimizes cell and I/O placement for best fit
 - Eases conversion from other PLD designs
- **Translation to PLACE Source File**
 - Optionally creates PLACE ".psf" source file
 - Allows architectural viewing of design
 - Alternate compiler for complex designs
 - JEDEC file waveform simulator
- **PEEL Array ABEL Design Examples**
 - Numerous examples provided for reference
 - Combinatorial, synchronous, asynchronous applications
- **System Requirements**
 - PC compatibles (DOS 5.0 or greater)
 - Sun SPARCstations (Contact ICT)

5

General Description

The ABEL-to-PEEL Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using the ABEL 4.0 (or greater) high-level design language from Data I/O. The ABEL development methodology is fully maintained through design entry, compilation and functional simulation. The fitter operates on "Berkeley Espresso" PLA files that are produced by the ABEL compiler and creates PEEL Array JEDEC programming files. The ABEL-to-PEEL Advanced Device Fitter provides true independent design entry; therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or preset nodes. The fitter automatically opti-

mizes the placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the configuration selected by the fitters is stored in a ".log" file. The fitter also allows use of the PLACE software by optionally creating a ".psf" extension file which allows architectural viewing of the design in PLACE software. This makes it possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array ABEL design examples using combinatorial, synchronous and asynchronous designs are provided for reference. The ABEL-to-PEEL Fitter operates on PC compatibles with DOS 5.0 or Sun SPARCstations.

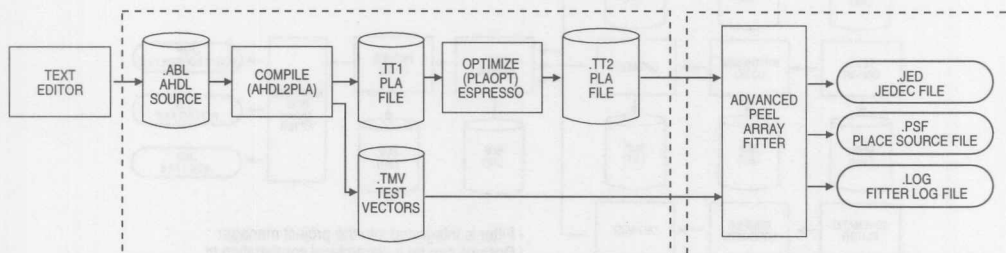


Figure 1. Design flow with the ABEL-to-PEEL Advanced Fitter

Synario®/ABEL-to-PEEL™ (for Windows) Advanced Device Fitter

Features

- **PEEL Array Support for Synario**
 - Supports PA7024, PA7128 and PA7140
 - Operates with Synario 2.0 or greater
- **Maintains Synario Design Methodology**
 - Design, compile, simulate with Synario
 - Fitter creates JEDEC programming files
 - Supports schematic and HDL entry
- **True Device-Independent Design Entry**
 - I/O pin and node numbers need not be specified
 - Optimizes cell and I/O placement for best fit
- **Translation to PLACE Source File**
 - Optionally creates PLACE ".psf" source file
 - Allows architectural viewing of design
 - Alternate compiler for complex designs
 - JEDEC file waveform simulator
- **PEEL Array Synario Design Examples**
 - Numerous examples provided for reference
 - Schematic and Synario HDL designs included
- **System Requirements**
 - IBM-compatible PCs

General Description

The Synario-to-PEEL Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using Synario 2.0. The Synario development methodology is fully maintained through design entry, compilation and functional simulation. Designs can be described using schematics and text in Data I/O's ABEL industry-standard format, or VHDL. The fitter operates on BLIF files that are produced by the Synario compiler, and creates PEEL Array JEDEC programming files. The Synario-to-PEEL Advanced Device Fitter provides true independent design entry; therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or preset

nodes. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the fitting results is recorded in the .log (report) file. The fitter also allows use of ICT's PLACE software by optionally creating a ".psf" extension file which allows architectural viewing of the design in PLACE. It is also possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array Synario schematic, ABEL, and VHDL design examples are provided for reference. The Synario-to-PEEL Fitter operates on IBM-compatible 386, 486, or 586 PCs.

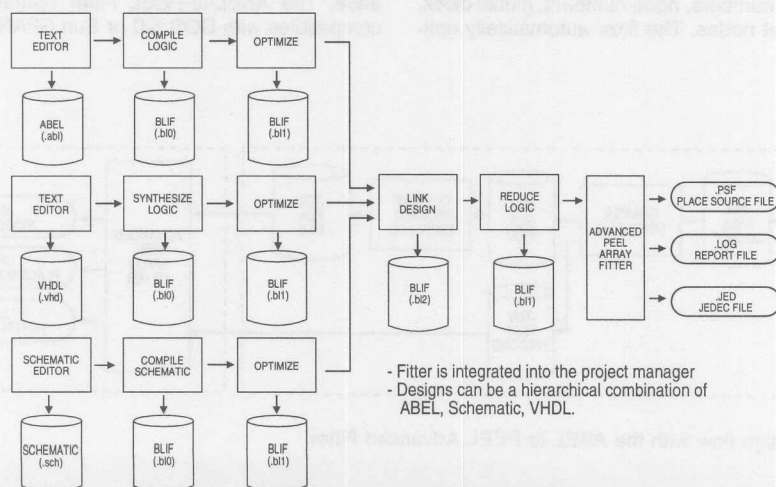


Figure 1. Flow diagram for Synario.

CUPL-to-PEELTM Advanced Device Fitter

Features

- **PEEL Array Support for CUPL Software**
 - Supports PA7024, 7128 and 7140
 - Operates with CUPL 4.5 or greater
- **Maintains CUPL Design Methodology**
 - Design, compile, simulate with CUPL
 - Fitter creates JEDEC programming files
 - Operates on "Berkeley Espresso" PLA files
- **True Device Independent Design Entry**
 - I/O pin and node numbers need not be specified
 - Optimizes cell and I/O placement for best fit
 - Eases conversion from other PLD designs
- **Translation to PLACE Source File**
 - Optionally creates PLACE ".psf" source file
 - Allows architectural viewing of design
 - Alternate compiler for complex designs
 - JEDEC file waveform simulator
- **PEEL Array CUPL Design Examples**
 - Numerous examples provided for reference
 - Combinatorial, synchronous and asynchronous applications
- **System Requirements**
 - PC compatibles (DOS 5.0 or greater)

5

General Description

The CUPL-to-PEEL Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using the CUPL 4.5 (or greater) high-level design language from Logical Devices. The CUPL development methodology is fully maintained through design entry, compilation and functional simulation. The fitter operates on "Berkeley Espresso" PLA files that are produced by the CUPL compiler and creates PEEL Array JEDEC programming files. The CUPL-to-PEEL Advanced Device Fitter provides true independent design entry; therefore, it is not necessary to specify pin numbers, node numbers, global clock, reset or pre-set nodes. The fitter automatically optimizes the

placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the configuration selected by the fitters is stored in a ".log" file. The fitter also allows use of the PLACE software by optionally creating a ".psf" extension file which allows architectural viewing of the design in PLACE software. This makes it possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array CUPL design examples using combinatorial, synchronous and asynchronous designs are provided for reference. The CUPL-to-PEEL Fitter operates on PC compatibles with DOS 5.0 or greater.

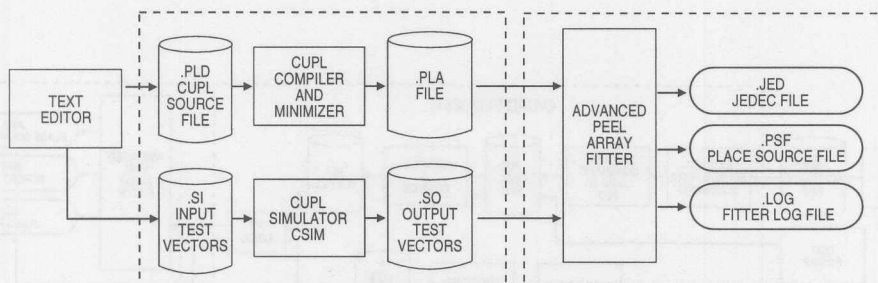


Figure 1. Design Flow for the CUPL-to-PEEL Advanced Fitter

OrCAD[®]-to-PEEL[™] Advanced Device Fitter

Features

- **PEEL Array Support for OrCAD PLD 386+**
 - Supports PA7024, PA7128 and PA7140
 - Operates with OrCAD PLD 386+ 2.0 or greater
- **Maintains OrCAD Design Methodology**
 - Design, compile, simulate with OrCAD
 - Fitter creates JEDEC programming files
 - Supports schematic and HDL entry
- **True Device-Independent Design Entry**
 - I/O pin and node numbers need not be specified
 - Optimizes cell and I/O placement for best fit
 - Extensive library of gate and TTL functions
- **Translation to PLACE Source File**
 - Optionally creates PLACE ".psf" source file
 - Allows architectural viewing of design
 - Alternate compiler for complex designs
 - JEDEC file waveform simulator
- **PEEL Array OrCAD Design Examples**
 - Numerous examples provided for reference
 - Schematic and OrCAD HDL designs included
- **System Requirements**
 - IBM- or NEC-compatible 386 or 486 PCs running DOS

General Description

The OrCAD-to-PEEL Advanced Device Fitter allows designers to create programming files for ICT's PEEL Array family (PA7024, PA7128, PA7140) using OrCAD PLD 386+ Programmable Logic Design Tools. The OrCAD development methodology is fully maintained through design entry, compilation and functional simulation. Designs can be described using schematics from OrCAD SDT 386+, text in OrCAD's OHDL format, or any combination of the two. The fitter operates on "Berkeley Espresso" PLA files that are produced by the OrCAD compiler, and creates PEEL Array JEDEC programming files. The OrCAD-to-PEEL Advanced Device Fitter provides true independent design entry; therefore, it is not necessary to specify pin numbers, node numbers,

global clock, reset or preset nodes. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit. This feature eases the conversion from other PLD designs. A detailed description of the fitting results is recorded in the .rpt (report) file. The fitter also allows use of ICT's PLACE software by optionally creating a ".psf" extension file which allows architectural viewing of the design in PLACE. It is also possible to simulate test vectors stored in the JEDEC file while using the PLACE software. Numerous PEEL Array OrCAD schematic and OHDL design examples are provided for reference. The OrCAD-to-PEEL Fitter operates on IBM- or NEC-compatible 386 or 486 PCs running DOS.

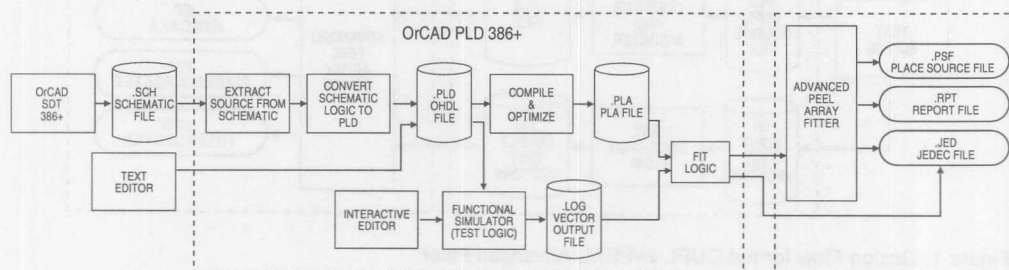


Figure 1. OrCAD design process for PEEL Arrays.

PDS-3 PEELTM Development System

Features

- **Development System for PEEL Products**
 - PLACE Advanced Development Software
 - PDS-3 Programmer
- **Design from Concept to Silicon**
 - Editor, logic compiler, simulator, translator, programmer, tester in one system
- **Supports PEEL Devices and PEEL Arrays**
 - PEEL 16V8, 18CV8, 20V8, 22CV8, 20CG10A, 22CV10A
 - PA7024, PA7128, and PA7140
- **Handles DIP, PLCC, SOIC, and TSSOP Packages**
 - Standard 40-pin 300-600mil DIP ZIF socket
 - Optional PLCC, SOIC and TSSOP adapters
- **Programmer Functions**
 - Program, read, verify, secure
 - Functional test via JEDEC file vectors
 - Checksum, position and continuity check, blank check, illegal-bit check, auto-sense
- **Translate Standard PLDs to PEEL Devices**
 - Reads most PLDs (e.g., PAL, GAL, EPLD)
 - PLACE translator automatically converts design for programming PEEL Devices
- **System Requirements**
 - IBM PC compatible with DOS 3.0 or greater
 - 640K bytes RAM minimum
 - Serial port for programmer upload/download

General Description

The PEEL Development System (PDS-3) is a powerful, yet inexpensive, PC-based system for designing with Programmable Electrically Erasable Logic (PEEL) products. Equipped with ICT's PLACE Development Software (see PLACE data sheet), the PDS-3 programmer has everything needed to create PEEL Device/Array designs from concept to silicon. The standard 40-pin DIP zero-insertion-force socket handles DIP packages from 20 to 40 pins, as well as PLCC, SOIC and TSSOP packages using optional adapters. All standard programming functions are supported including: program, read, verify and secure. Test vectors from the JEDEC file can be applied to the device for functional verifica-

tion. Built-in features ensure device integrity and reliable programming including: checksum, position/continuity check, blank check, and illegal-bit check. The auto-sense features automatically activates the PDS-3 in response to the socket without any key presses. The PDS-3 can read most any PLD (e.g., PAL, GAL, EPLD) for conversion to a PEEL Device using the PLACE translator. System requirements include an IBM PC compatible computer with DOS 3.0 or greater, 640K RAM and serial port. Note: the PDS-3 can be upgraded to a universal PLD and memory programmer, contact ICT for more information.

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Figure 1. PDS-3 Development System

ICT Inc. PEEL Array Programming Support

Company	Telephone	Product	PA7024	PA7128	PA7140
Advantech Corp.	(408) 245-6678	PC-UPROG	V.1.8	V.1.9	V.1.9
Advin Systems	(408) 243-7000	PILOT-U40-U84	V.10.03	V.10.77	V.10.77
BP Microsystems	(800) 225-2102	BP1100	V.1.53	V.2.30	V.2.31
BP Microsystems	"	BP1128	V.1.53*	V.2.30*	V.2.31*
BP Microsystems	"	BP1200	V.1.53*	V.2.30*	V.2.31*
Bytek	(407) 994-3520	U135HFT-U/A	V15	C.F.	C.F.
Data I/O Corp.	(800) 426-1045	2900	V.1.6*	V.3.3*	V.3.6
Data I/O Corp.	"	3900	V.1.0*	V.2.3*	V.2.6
Data I/O Corp.	"	Unisite	V.3.2*	V.4.4*	V.4.8
Data I/O Corp.	"	Autosite	V.1.0*	V.2.3*	V.2.6
Data I/O Corp.	"	Chip-Lab	V.1.0*	V1.2*	C.F.®
Electronic Engr. Tools	(408) 734-8184	All-Max	V.1.0	V.1.0	C.F.
Hi-Lo Research Co.	011-88627640215	All-07	V.3.08	V.3.08	V.308
ICT, Inc.	(408) 434-0678	PDS-3	V.1.00*	V.1.01*	V.1.01*
Logical Devices, Inc.	(305) 974-0967	Allpro 40-88	V.2.1	V.2.4	V.2.4
Logical Devices, Inc.	"	Allpro 88XR	V.1.34	V.1.34	V.1.34
Logical Devices, Inc.	"	ChipMaster	V.1.8	V.1.9	V.1.9
SMS	(206) 883-8447	Optima	#C3/92*	#C/93*	#A/94*
SMS	"	Expert	#C3/92	#C/93	#A/94
SMS	"	Plus48	#C3/92	#C/93	#A/94
Stag Microsystems	(408) 988-1118	Eclipse	V.2.5	V.2.3	C.F.
System General	(408) 263-6667	Turpro1/FX	V.1.68*	V.1.68K*	V.1.68K*
Tribal Microsystems	(510) 623-8859	FLEX-700	V.3.08	V.3.08	V.3.08
Xeltek	(408) 524-1929	Superpro II	V.1.0	V.1.7C	V.1.7C

C. F. = Call Factory, ICT 1-800-SAY-PEEL (1-800-729-7335)

Note *: The programming algorithm has been qualified by ICT as of 12/15/94. For all others, contact ICT for latest status.

Note ®: This device's algorithm is available on Data I/O's BBS (as an extended algorithm) or on Data I/O's Keep Current Express, call ICT or Data I/O for more information.

Newly-released versions of programming algorithms can be downloaded from the following BBSs:

ICT Inc.: BBS 408-434-0130 (14,400bps, N, 8, 1)

BP Microsystems: BBS 713-688-9283

Logical Devices: BBS 315-428-8014

DATA I/O: Keep Current Express (USA) 206-881-3465, (UK) +44-734-444-8914, (Germany) +49-89-858-5880, (Japan) +81-33-436-0205, Public BBS 206-882-3211

ICT Inc. PEEL Device Programming Support

Company	Telephone	Product	PEEL16V8	PEEL18CV8	PEEL20V8	PEEL22CV8	PEEL20CG10A	PEEL22CV10A®	PEEL22CV10A+
Advantech Corp.	(408) 245-6678	PC-UPROG	(V.2.35)	V.2.0*	(V.2.35)	V.2.3	V.1.7*	V.1.2*	V.1.2*
Advin Systems	(408) 243-7000	PILOT-U40-U84	C.F.	V.10.78*	C.F.	C.F.	V.10.50*	V.9.94*	V.9.94*
BP Microsystems	(800) 225-2102	BP1100	C.F.	V.2.31*	C.F.	C.F.	V.2.19*	V.1.53*	V.1.53*
BP Microsystems	"	BP1128	C.F.	V.2.31*	C.F.	C.F.	V.2.19*	V.1.53*	V.1.53*
BP Microsystems	"	BP1200	C.F.	V.2.31*	C.F.	C.F.	V.2.19*	V.1.53*	V.1.53*
Bytek	(407) 994-3520	U135HFT-U/A	C.F.	V.59	C.F.	C.F.	V.59	V.15*	V.15*
Data I/O Corp.	(800) 426-1045	2900	V3.6	V.3.3*	V.3.6	V.3.6	V.3.0*	V.3.6	V.3.6
Data I/O Corp.	"	3900	V2.6	V.2.3*	V.2.6	V.2.6	V.3.0*	V.2.6	V.2.6
Data I/O Corp.	"	Unisite	V4.8	V.4.4*	V.4.8	V.4.8	V.4.0*	V.4.8	V.4.8
Data I/O Corp.	"	Autosite	V2.6	V.2.3	V.2.6	V.2.6	V.2.3	V.2.6	V.2.6
Data I/O Corp.	"	Chip-Lab	C.F.	V1.20	C.F.	C.F.	V.1.01	V.1.00	V.1.00
Electronic Engr. Tools	(408) 734-8184	All-Max	C.F.	(V.1.4)	C.F.	C.F.	V.1.4	V.1.4	V.1.4
Hi-Lo Research Co.	011-88627640215	All-07	C.F.	V.3.34	C.F.	V.3.36A	V.1.0	V.1.0	V.1.0
ICT, Inc.	(408) 434-0678	PDS-3	V.1.18*	V.1.3*	V.1.19*	V.1.18*	V.1.00*	V.1.00*	V.1.00*
Logical Devices, Inc.	(305) 974-0967	Allpro 40-88	Q1/95	V.2.4*	Q1/95	Q1/95	V.2.3*	V.2.2*	V.2.2*
Logical Devices, Inc.	"	Allpro 88XR	Q1/95	V.1.34	Q1/95	Q1/95	V.1.31*	V.1.0*	V.1.0*
Logical Devices, Inc.	"	ChipMaster	(V.2.35)	V.2.0	(V.2.35)	V.2.3	V.1.9	V.1.2	V.1.2
SMS	(206) 883-8447	Optima	B9/94	#C1/93	C.F.	C.F.	#3/92	#3/92	#3/92
SMS	"	Expert	B9/94	#C1/93	C.F.	C.F.	#3/92	#3/92	#3/92
SMS	"	Plus48	B9/94	#C1/93	C.F.	C.F.	#3/92	#3/92	#3/92
Stag Microsystems	(408) 988-1118	Quasar 1040/1084	Q1/95	stPAL	Q1/95	Q1/95	stV	stV	stV
System General	(408) 263-6667	Turpro1/FX	(V.2.15)	V.2.07*	V.2.21*	(V.2.15)	V.1.68*	V.1.68*	V.1.68*
Tribal Microsystems	(510) 623-8859	FLEX-700	C.F.	V.3.34	C.F.	V.3.36A	V1.0	V.1.0	V.1.0
Xeltek	(408) 524-1929	Superpro II	V.2.01	V.1.7C*	Q1/95	Q1/95	V.1.7A*	V.1.0*	V.1.0*

C. F. = Call Factory, ICT 1-800-SAY-PEEL (1-800-729-7335)

Note *: The programming algorithm has been qualified by ICT as of 12/15/94. For all others, contact ICT for latest status.

Note @: The PEEL22CV10AJ-5 (5ns PLCC) devices may require a special DIP-to-PLCC programming adapter from ICT.

Note @: The device's algorithm is available on Data I/O's BBS (as an extended algorithm) or on Data I/O's Keep Current Express, call ICT or Data I/O for more information.

Newly-released versions of programming algorithms can be downloaded from the following BBSs:

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DATA I/O: Keep Current Express (USA) 206-881-3465, (UK) +44-734-444-8914, (Germany) +49-89-858-5880, (Japan) +81-33-436-0205, Public BBS 206-882-3211

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Logical Design Techniques for PEEL™ Devices

Architectural Enhancements

Designing with PEEL Devices is much like designing with other 20 or 24-pin SPLDs. However, superset PEEL Devices (such as the PEEL18CV8, 22CV8, 20CG10A and 22CV10A) give designers greater flexibility with additional inputs, product terms and macrocell configurations. The following information describes some of the design benefits of PEEL Device enhanced architectures.

Independent Output Enables

Each I/O has independent programmable output enables for both combinatorial or registered outputs. The output enables are helpful for bus interfacing as well as "wire-ORing" of signals. Each I/O can be enabled or disabled via individual product terms, even on registered outputs where most standard PLDs offer only a single output enable control pin.

Global Preset and Clear

The PEEL18CV8, 22CV8, 20CG10A, 22CV10A and 22CV10AZ each have a synchronous preset (SP) and asynchronous clear (AC) product term that control all the registers. Although these functions are fairly straight forward, there are some unique ways to take advantage of them, especially for counters and state machines. An example is shown in the 8-bit Counter with Function Controls design in the application section of this note.

Twelve-Configuration Macrocell

All of ICT's superset SPLDs have a twelve-configuration macrocell as shown in Figure 2. Macrocell configuration numbers 3, 4, 9 and 10 (shaded in Figure 1) are the four macrocell configurations most similar to the standard SPLDs such as the 16V8 and 20V8. The additional eight macrocell configurations can be used for a variety of logic functions not possible with ordinary SPLDs.

Bi-Directional Registered I/O

Two of the additional PEEL macrocell configurations include bi-directional registered I/O both active-high and active-low (#1 and #2 in Figure 1). The difference between this configuration and the registered

Contents

Architectural Enhancements

- Independent Output Enables
- Global Preset and Clear
- Twelve-Configuration Macrocell
- Bi-Directional Registered I/O
- Buried Combinatorial Feedback
- Buried Combinatorial Feedback with Register
- Buried Register with Combinatorial Output

Design Tricks and Techniques

- Input Synchronizer (Buried Latch)
- Bus-Programmable Multiplexer
- Change-of-State Detect (Buried Register)
- 8-Bit Counter with Function Controls
- Faster Delays with Internal Feedback

6

output of standard PLDs (e.g., 16R8) is that the feedback is from the pin rather than the register. This makes it possible to use a registered output as an input also. Some possible applications for this include: synchronous-read/writable I/O, bus interfaced code conversion, and the wired-OR "Busy" function for bus arbitration circuits.

Buried Combinatorial Feedback

Two additional macrocell configurations found in PEEL devices allow for buried combinatorial feedback before the output enable (#7 and #8 in Figure 1). This configuration is very useful for creating latches or logic paths that must be used internally, but only appear externally when accessed by the processor (i.e., as when interfaced to a bus). Furthermore, this configuration is useful in reducing propagation delays when feeding an output signal back into the device for another logic function. This is because the signal is routed directly into the array rather than delayed through the I/O buffer at the pin. An example of how buried combinatorial feedback can be used is shown in the "Change-of-State Detector" application in the following section.

Buried Combinatorial Feedback with Register

Two other PEEL macrocell configurations provide buried combinatorial feedback with a registered output (#5 and #6 in Figure 1). This configuration lends

itself to clock synchronization applications. In such applications the buried combinatorial feedback can create an asynchronous latch, the output of which will be stable for clocking into the register. This circuit can be used for interfacing data between two systems operating from different clocks or for simply synchronizing asynchronous signals.

Buried Register with Combinatorial Output

Another useful macrocell configuration is the pseudo-buried register with combinatorial output (#11 and #12 in Figure 1). This configuration allows the register output to be fed back into the array while the combinatorial function is routed to the pin. This configuration makes it possible to use the registers as programmable buried storage nodes while the outputs can be selectively addressed for reading

onto a bus. Possible functions or applications for this configuration include: programmable comparator, programmable dip-switch, buried control register, programmable mask register. An example of how this configuration is used can be seen in the "Change-of-State Detector" application in the following section.

Design Tricks and Techniques

The following application examples demonstrate a few of the many possible ways to use the enhanced architectures of PEEL Devices. All of the examples were designed using ICT's PLACE Development Software and are included with the software.

Input Synchronizer (Buried Latch)

Quite often systems need to synchronize an asynchronous input in order to avoid potential metastabil-

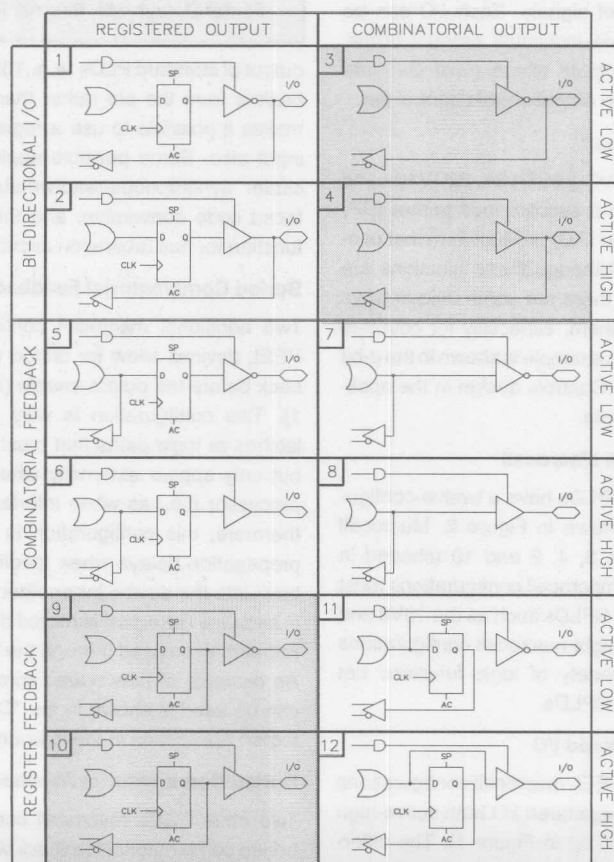


Figure 1. PEEL Device 12-Configuration Macrocell.

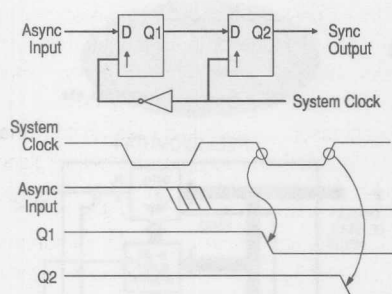


Figure 2. Input synchronizer with standard logic.

ity conditions caused by set-up time violations. A common way of doing this uses two cascaded D-type flip-flops (i.e. 74LS74) as shown in Figure 2. In this circuit the asynchronous input is fed into the D input of the first flip-flop. The Q output is then fed into the D input of the second. The resulting Q output of the second flip-flop will be synchronized to the clock.

PEEL devices can implement the same type of circuit with only one input pin, one macrocell and a system clock. This is done by using the internal feedback with register macrocell configuration (5 or 6 in Figure 1). The PEEL circuit, shown in Figure 3, is made of a buried gated-latch that internally latches the asynchronous input on the falling edge of the clock. This holds the input stable to meet the set-up time of the register which is clocked on the rising edge. If the input violates the set-up time of the gated-latch, the

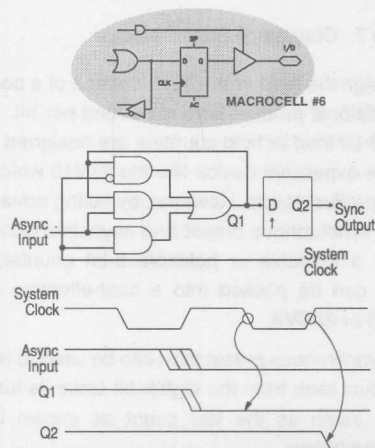


Figure 3. Input synchronizer with PEEL Device.

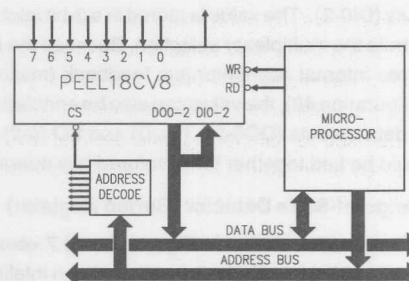


Figure 4. Bus-Programmable Multiplexer System

clock low time will resolve possible metastability in time for the high-going register clock. The equations for the latch are shown below.

$Q2 := CLK \ \& \ IN \ \# \text{"when CLK=1 allow input to set-up"}$

$ICLK \ \& \ Q2 \ \# \text{"when CLK=0 latch input internally"}$

$IN \ \& \ Q2 \ \text{"prevent hazard condition"}$

If multiple input synchronizers are needed for a system, the PEEL device solution becomes even more elegant. This is because only two pins per synchronizer are needed. Thus, a PEEL18CV8 could implement eight such synchronizer circuits in a single 20-pin package.

Bus-Programmable Multiplexer

This application (shown in Figures 4 and 5) implements an 8 to 1 multiplexer that can be interfaced to a μP bus. Any one of the 8 Inputs (I0-7) can be selectively routed to the output (OUT) by writing (/WR and /CS=0) a 3-bit binary value to the data

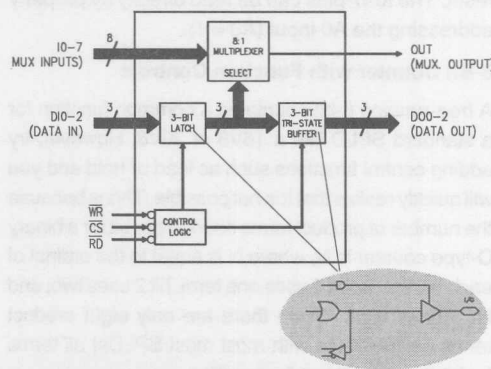


Figure 5. Buried Latches in Bus-Programmable Multiplexer

inputs (DI0-2). The value is stored in a 3-bit latch that controls the multiplexer selection. Because the latch utilizes internal asynchronous feedback (macrocell configuration #8), the value can also be enabled onto the data outputs (DO0-2). The DI and SO (0-2) pins should be tied together for write/read bus operation.

Change-of-State Detector (Buried Register)

The application shown in Figures 6 and 7 uses the PEEL22CV10A (with the "+" option) as an intelligent input port that off-loads the μ P from software polling. The change-of-state detector incorporates eight inputs that are monitored for a change-of-state (low or high). An 8-bit comparator compares the current input state with the last one which is stored in eight pseudo-buried registers using macrocell configuration 12. If a change occurs an interrupt will be asserted. The μ P can then read either the eight pseudo buried registers holding the change-of-state or read the input pins directly. Uses for such a circuit include: sensor monitoring, "glitch" detection, handshaking and clock synchronization.

The operation of the Change-of-State Detection Port is as follows: any change on the inputs (low-to-high or high-to-low) can be detected via an 8-bit non-equality comparator (NEQ). When detected, the INTR latch output is set for interrupting a μ P. The INTR output is also used to clock the 22CV10A+ which latches the input state into eight pseudo-buried registers. The μ P can then read the registers on D0-D7 when CS, RD, and A0 = 0. Once read (unless another change has occurred) the INTR latch will be reset. The I0-I7 pins can be read directly by properly addressing the A0 input (A0 = 1).

8-Bit Counter with Function Controls

A free-running 8-bit counter is a common function for a standard SPLD like a 16V8 or 20V8. However, try adding control functions such as load or hold and you will quickly realize that it is not possible. This is because the number of product terms needed per bit for a binary D-type counter is N, where N is equal to the ordinal of each bit, that is, bit 1 uses one term, bit 2 uses two, and bit 8 uses eight. Since there are only eight product terms per SUM (as with most most SPLDs) all terms for bit-8 are used just for counting.

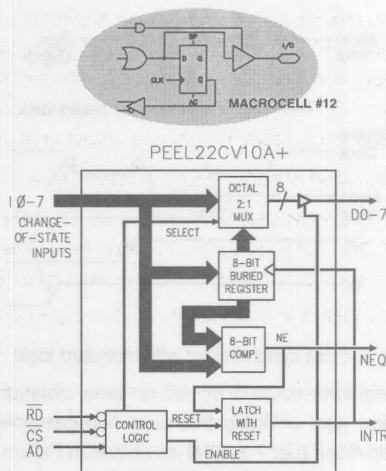


Figure 6. PEEL22CV10A+ Change-of-State Detector functional block diagram.

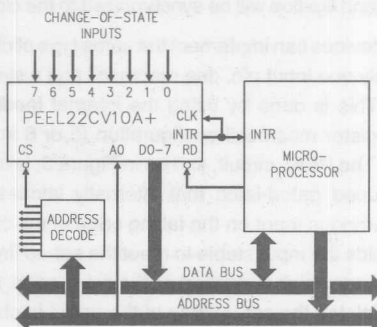


Figure 7. Change-of-State Detector

To design the load or the hold function of a counter, an additional product term is needed per bit. Thus, most 8-bit load or hold counters are designed using a more expensive device like the 22V10 which has more product terms. However, by taking advantage of the synchronous preset and asynchronous clear terms, a loadable or holdable 8-bit counter, plus more, can be packed into a cost-effective PEEL 18CV8 or 22CV8.

The synchronous preset term can be used to free up a product term from the eighth bit since its function is the same as the last count as shown in the equation below.

$$SP := Q7 \& Q6 \& Q5 \& Q4 \& Q3 \& Q2 \& Q1 \& !Q0$$

Freeing this product term from the eighth bit allows room for the load or hold function. An example of a multi-function 8-bit counter designed into an 18CV8 is shown in Figure 8. The counter has four control functions: hold, reset, repeat and output enable.

The operation of each control is listed below.

SYNCHRONOUS RESET - When set high, the outputs (Q0-7) will go low after the next clock. When set low, the counter will start counting up with each clock.

HOLD COUNT - When set high, the count will hold the present state. When low, the count will resume.

REPEAT COUNT - When set high, the counter will repeat the count after reaching FF_{HEX}. When set low, the counter stops after one complete count. The asynchronous clear product term is used for this function.

OUTPUT ENABLE - When high, the outputs will be disabled and will enter a high impedance state. When low, the outputs are enabled.

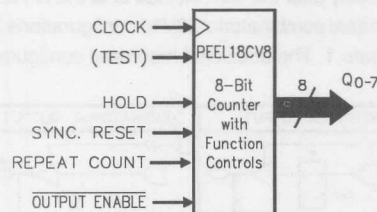


Figure 8. 8-bit Counter with Hold and other function controls using preset P-term.

All preceding applications were created using the PEEL Development System with the PLACE™ logic compiler. For more detailed information on these and other applications refer to the ICT PLACE Software Users Manual.

Using Internal Timing of PEEL Devices

Introduction

ICT's CMOS Programmable Electrically Erasable Logic (PEEL) devices are flexible simple PLDs with external speed performance as fast as 5ns t_{pd}. In addition to the high performance, PEEL devices provide low-power, reprogrammability and additional macrocell configurations. The additional macrocell configurations not only add functionality but also further enhance performance.

The unique internal feedback macrocell configuration offers fast internal propagation delays. For example, a 22CV10A-10 has an internal t_{PD1} of 7ns. This makes it possible to achieve internal multi-level logic functions over 3ns faster per level than any other 10ns 22V10. The same applies for other PEEL devices as well, though the PEEL 22CV10A-10 will be used as an example. Internal timing for the PEEL 18CV8, 20CG10A and 22CV10A is provided at the end of this application note.

Internal Combinatorial Timing

System designers using programmable logic devices to implement functions such as range decoders, adders, arithmetic logic, parity generator/checkers, etc., often encounter limitations due to the number of product terms available per sum. For example, the carry-out function for a four-bit, carry-look-ahead adder requires over 36 product terms, while the most significant bit requires 28 product terms. An n -bit parity generator/checker requires 2^{n-1} product terms. Such logic applications are almost impossible to directly map into standard sum-of-product PLDs.

A common solution for fitting these applications into a standard PLD is to use multi-level logic design. The penalties of using this method are the effective loss of I/Os and the added propagation delay of a second level of logic. Most standard PLD manufacturers provide an external propagation delay specification called t_{PD} . To obtain the total propagation delay of a multi-level logic circuit, simply multiply the device t_{PD} by the number of logic levels used. Thus a device with 10ns t_{PD} would require 20ns for two levels, 30ns for three levels, and so on.

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PEEL Macrocells for Multi-level Logic

Multi-Level Logic Application

Internal Sequential Timing

Internal Timing Specifications

PEEL Macrocells for Multi-level Logic

ICT's PEEL22CV10A provides additional macrocell configurations which allow designers to achieve faster propagation delay for multi-level logic by using internal tpd timing (configurations 5-8 in Figure 1). Notice that these four macrocell configurations allow for feedback immediately after the sum instead of at the pin as with the standard combinatorial 22V10 configurations 3 and 4 in Figure 1. The additional macrocell configurations

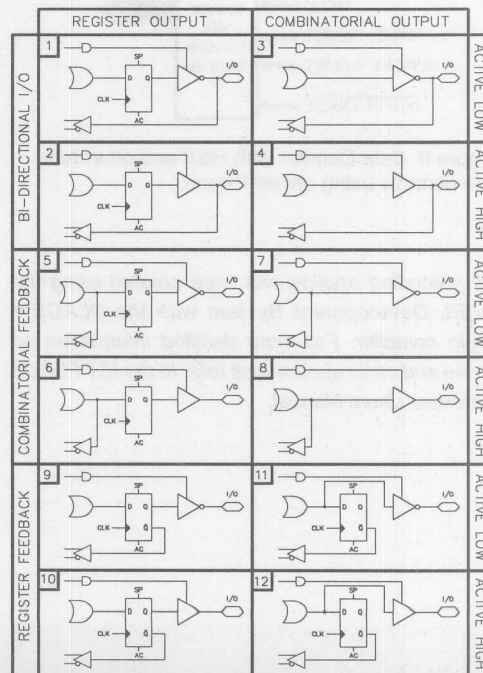
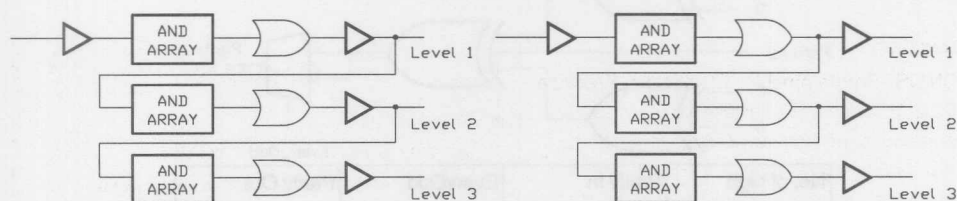


Figure 1. PEEL22CV10A Macrocell Configurations



Standard 22V10 - External Feedback Path

PEEL22CV10A - Internal Feedback Path

	Standard 22V10-10	Propagation Delay
level 1	t_{PD}	10 ns
level 2	$2x(t_{PD})$	20 ns
level 3	$3x(t_{PD})$	30 ns

	PEEL 22CV10A-10	Propagation Delay
level 1	t_{PD}	10 ns
level 2	$t_{PD} + t_{PDI}^*$	17 ns
level 3	$t_{PD} + 2x(t_{PDI})^*$	24 ns

* t_{PDI} = Internal propagation delay = 7ns

 Figure 2. Multi-level Logic in Standard 22V10-10 vs PEEL22CV10A-10 with Internal t_{PDI}

can be used by specifying the 22CV10A+ as the device type in the design source file. Programming is accomplished also by specifying the 22CV10A+.

Figure 2 shows the circuit and timing differences for external and internal timing of the 22CV10A-10. With its 7ns internal timing " t_{PDI} ", the PEEL22CV10A removes the additional delay caused by the output buffer making it the best candidate for high speed multi-level logic design.

Multi-level Logic Application

This application uses the PEEL22CV10A as a 9-bit even/odd parity generator/checker. The application takes advantage of the PEEL22CV10A's internal timing and saves at least 3ns in comparison to an implementation in a standard 22V10 device. A functional diagram of a 9-bit parity even/odd generator/checker is shown in Figure 3 and the corresponding table lists its functional operation.

The parity function is commonly implemented via the utilization of the exclusive-OR operation. To build an n-bit parity generator/checker, the number of 2-input

exclusive-OR gates required is $n-1$. An n-bit parity function can also be implemented via the AND-OR logic operation but it requires 2^{n-1} product terms. For instance, a 9-bit parity function will require 256 product terms. Though the PEEL22CV10A device has only 132 product terms, a 9-bit parity function can still be implemented by using two macrocells to implement two 4-bit parity generators. Both outputs of the macrocells are fed back and XORed with the 9th bit (Parity_In). With this method, there is an additional delay due to the feedback of the 4-bit parity generator outputs. If this design is implemented in the PEEL22CV10A device, the delay is about 3ns less than if it were implemented in a standard 22V10 device. This is because the outputs in the 22V10 device are fed back from the pin, whereas in the PEEL22CV10A the outputs can be configured to feedback directly from the OR gate (before the output buffer).

The design file implementation of the PEEL22CV10A as a 9-bit parity generator/checker is included with ICT's PLACE Development Software.

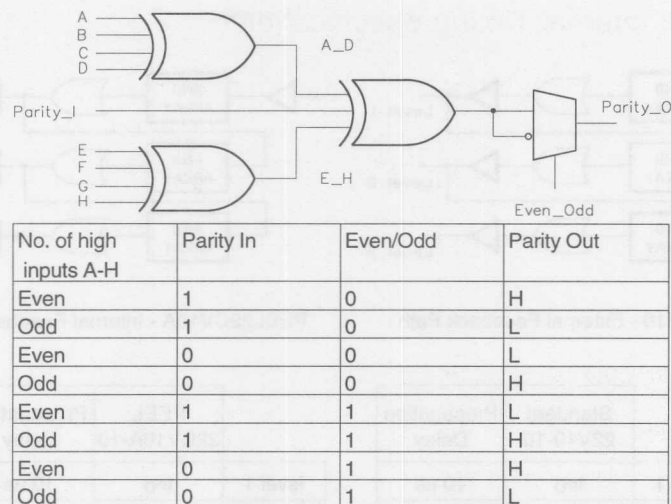


Figure 3. 9-Bit Parity Even/Odd Generator/Checker

Internal Sequential Timing

The maximum frequency for sequential logic functions, such as counters and state-machines, is typically calculated for the 22CV10A-10 as follows:

$$f_{MAX} = 1/(t_{sc} + t_{co})$$

$$f_{MAX} = 1/(5ns + 6ns) = 90.9MHz$$

Where t_{sc} is the input set-up-to-clock and t_{co} is clock-to-output. This calculation assumes that the feedback could possibly be coming from an input pin (see Figure 4). In reality, many designs only use the internal feedback from the register and not any inputs (as shown in Figure 5). The ICT PEEL devices allow internal feedback from the register providing a high frequency of operation as shown below.

$$f_{MAX} = 1/(t_{sc} + t_{cf})$$

$$f_{MAX} = 1/(5ns + 4ns) = 111MHz$$

Even faster clocking can be accomplished with "pipelined" designs where feedback is not used at all. The timing in this configuration is just limited to the clock high and low time, providing proper set-up time is maintained (see Figure 6).

$$f_{MAX} = 1/(t_{cl} + t_{ch})$$

$$f_{MAX} = 1/(4ns + 4ns) = 125MHz$$

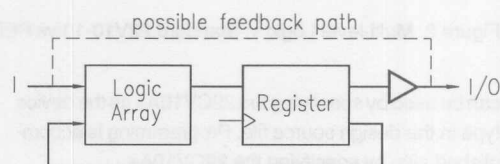


Figure 4. External feedback $f_{MAX} = 1/(t_{sc} + t_{co})$

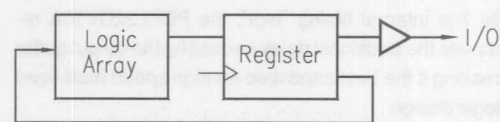
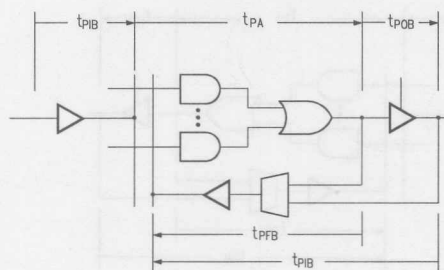


Figure 5. Internal Feedback $f_{MAX} = 1/(t_{sc} + t_{cf})$



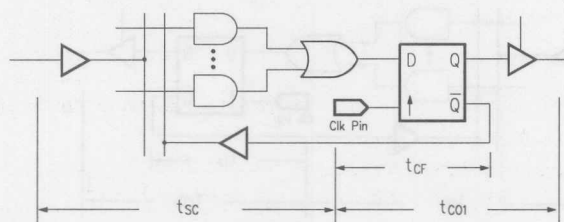
Figure 6. No feedback $f_{MAX} = 1/(t_{cl} + t_{ch})$

PEEL18CV8 Internal Timing Specification



PEEL18CV8 Internal Combinatorial Timing ^{4, 13}

Symbol	Parameter	-5	-7	-10	-15	-25	Unit
		Max	Max	Max	Max	Max	
t _{PIB}	Input or I/O pin to Input of Array	1.5	2	2.5	4	7	ns
t _{PFB}	Feedback to Input of Array	1.5	2	2.5	4	7	ns
t _{POB}	Output of Array to Output pin	1.5	3	3	5	5	ns
t _{PA}	Input of Array to Output of Array	2	2.5	4.5	6	13	ns
t _{PDI}	Internal propagation delay (t _{PA} +t _{PFB})	3.5	4.5	7	10	20	ns

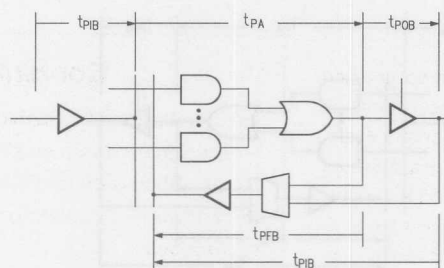
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PEEL18CV8 Internal Sequential Timing ^{4, 13}

Symbol	Parameter	-5		-7		-10		-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{SC}	Input or feedback setup to clock	3.5		5		5		12		20		ns
t _{CO1}	Clock to output		4		7		7		12		15	ns
t _{CO2}	Clock to combinational output delay via internal registered feedback		7.5		10		12		25		35	ns
t _{CF}	Clock to feedback		2.5		3.5		4		8		15	ns
t _{CL} , t _{CH}	Clock low time, clock high time	3		3.5		5		10		15		ns
f _{MAX1}	Max clock freq Int feedback (1/(t _{SC} +t _{CF}))	166.7		117.6		111		50		28.5		MHz
f _{MAX3}	Max clock freq No feedback (1/(t _{CL} +t _{CH}))	166.7		142.8		100		50		33.3		MHz

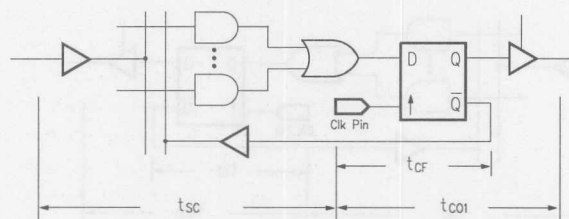
* Refer to the specific data sheets for description of footnotes

PEEL20CG10A and 22CV10A Internal Timing Specification



PEEL20CG10A/22CV10A Internal Combinatorial Timing ^{4, 13}

Symbol	Parameter	-5	-7	-10	-15	-25	Unit
		Max	Max	Max	Max	Max	
t _{PIB}	Input or I/O pin to Input of Array	1.5	2	2.5	4	7	ns
t _{PFB}	Feedback to Input of Array	1.5	2	2.5	4	7	ns
t _{POB}	Output of Array to Output pin	1.5	3	3	5	5	ns
t _{PA}	Input of Array to Output of Array	2	2.5	4.5	6	13	ns
t _{PDI}	Internal propagation delay (t _{PA} +t _{PFB})	3.5	4.5	7	10	20	ns



PEEL20CG10A/22CV10A Internal Sequential Timing ^{4, 13}

Symbol	Parameter	-5		-7		-10		-15		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{SC}	Input or feedback setup to clock	3		3		4		8		15		ns
t _{CO1}	Clock to output		4		5.5		6		8		15	ns
t _{CO2}	Clock to combinatorial output delay via internal registered feedback		7.5		10		12		17		35	ns
t _{CF}	Clock to feedback		2.5		3.5		4		5		9	ns
t _{CL} , t _{CH}	Clock low time, clock high time	2.5		3		5		6		13		ns
f _{MAX1}	Max clock freq Int feedback (1/(t _{SC} +t _{CF}))	181.8		142		111		76.9		41.6		MHz
f _{MAX3}	Max clock freq Int feedback (1/(t _{SC} +t _{CF}))	200		166		125		83.3		38.4		MHz

* Refer to the specific data sheets for description of footnotes

PEEL Device Metastability

Introduction to Metastability

Metastability is a type of failure that can occur when digital circuits attempt to synchronize asynchronous digital data. Whenever a clocked flip-flop synchronizes an asynchronous input (Figure 1), there is a small but finite probability that the output will exhibit an unpredictable response. This happens when the input transition violates the setup and hold time specification. In other words it actually occurs within the small timing window where the flip-flop decides to accept the new input. Under these circumstances the flip-flop enters an unstable intermediate state called metastable. A slight deviation from perfect balance will eventually cause the outputs to revert to one of the two stable states. But the settling time depends not only on the gain-bandwidth product of the circuit, but also on the original balance and the noise level of the circuit. Therefore, it can only be described in statistical terms.

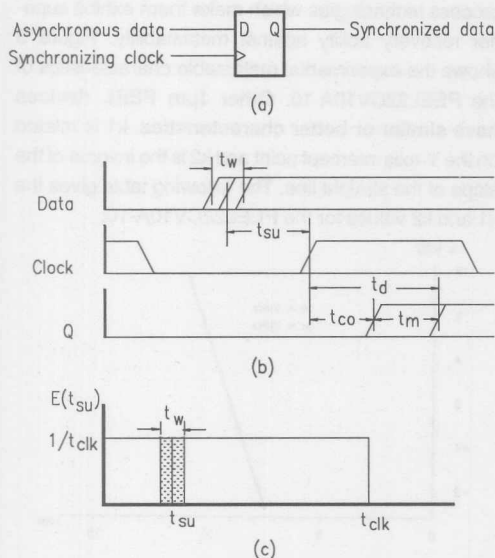


Figure 1. Single-stage synchronizer and definition of critical trigger window t_w

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Synchronizer Circuit Improves MTBF
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As shown in Figure 1, a critical trigger window t_w is defined. If a flip-flop timing constraint is violated during the time window t_w , the output Q is still unresolved within a decision time t_d . Referenced to the beginning of the trigger event which is the positive clock edge for the sample circuit in Figure 1, t_d thus includes the normal propagation delay t_{co} and extra delay due to metastability t_m . The relation $t_w = f(t_d)$ can be used for defining the metastable behavior of flip-flops. The exponential function was found to be asymptotically valid for the relation:

$$t_w = f(t_d) = a \cdot \exp(b \cdot t_d)$$

The probability density function for actual setup time $E(t_{su})$ is unity for one clock period t_{clk} (Figure 1). The probability for one data event to hit the critical window t_w is thus equivalent to the indicated area t_w/t_{clk} . With given $t_w(t_d)$ the reliability (mean time between failures, MTBF) of a synchronizer can be calculated to be:

$$MTBF(t_d) = 1 / (t_w(t_d) \cdot f_{CLK} \cdot f_{DATA})$$

We can rewrite the equation with the exponential relation:

$$MTBF = \exp(t_d/k_2) / (k_1 \cdot f_{CLK} \cdot f_{DATA})$$

k_1 and k_2 are constants we can get from experimental results to calculate MTBF with relative t_d , clock frequency f_{CLK} and data frequency f_{DATA} .

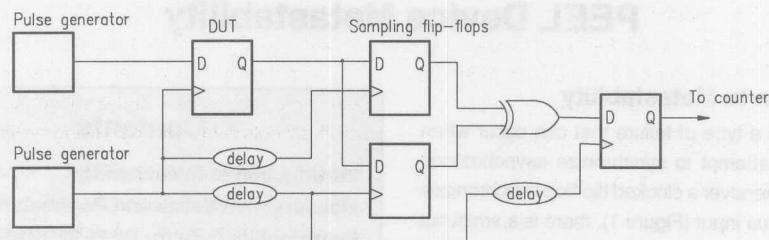


Figure 2. Metastability measurement setup

Measurement Setup and Parameters

Figure 2 shows a test circuit to measure metastable parameters of a synchronizer. A device under test (e.g. DUT) is triggered on its D and CLK inputs by two asynchronous free-running clocks. In this case, we use two different pulse generators to provide a data rate of 1 MHz and a clock rate of 2 MHz. The data transitions are randomly and evenly distributed over the entire clock period of about one transition per clock cycle. Under these circumstances, we may assume that the data transitions are also evenly distributed within the failure time window t_{ty} .

On the output of the DUT, there are two well characterized sampling flip-flops (the difference delay time via pin to D input and pin to CLK are characterized to prevent violation of setup time). These two flip-flops use the same clock signal used by the DUT; the first sampling clock is delayed by t_d (time delay for metastable output resolved t_d , and the second sampling clock is delayed by approximately 120 ns more. It is clocked so late that the probability that the output did not resolve at that time can be neglected.) Because this probability decreases exponentially with time, this condition can easily be satisfied.

The outputs of both sampling flip-flops are exclusive-ORed and the result sampled by another flip-flop with a fixed clock time delay. When the first two sample states differ, there must be a transition after t_{com} , revealing a late transition metastable condition on the DUT. Accumulating these pulses for some known time interval yields the MTBF of the DUT for a given t_{com} .

To run the test, t_{co} is used as a base delay (e.g. $t_{\text{M}}=0$). We get different MTBF with increasing t_{M} until MTBF is greater than 60 sec. When the MTBF results are plotted on semi-log paper, they yield a best-fit straight line with slope $-1/k_2$. k_1 then can be calculated by inserting a k_2 value into the MTBF equation. With k_1 and k_2 , the designer can easily find t_{com} for a chosen MTBF, f_{CLK} and f_{DATA} .

Metastability Data for PEEL22CV10A-10

ICT PEELs are based upon fast, CMOS EEPROM process technologies which make them exhibit superior recovery ability against metastability. Figure 3 shows the experimental metastable characteristics of the PEEL22CV10A-10. **Other 1 μ m PEEL devices have similar or better characteristics.** k_1 is related on the Y-axis intercept point and k_2 is the inverse of the slope of the straight line. The following table gives the k_1 and k_2 values for the PEEL22CV10A-10:

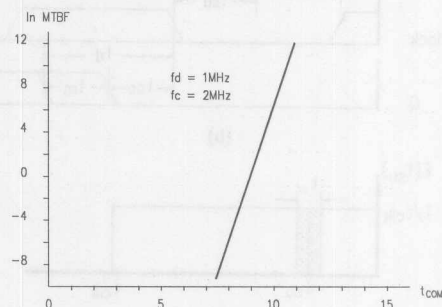


Figure 3. K2 plot of 22CV10A

Device	k_1	k_2
PEEL22CV10A-103x10110.16ns	3×10^{11}	0.16ns

For example, to determine the MTBF for the PEEL22CV10A-10 that is used as a synchronizer in a system with 33 MHz clock frequency, 25 MHz data rate, t_{MET} is calculated with the following equation:

$$t_{MET} = 1/f_{CLK} - t_{SU} - t_{CO} = 1/33 \text{ MHz} - 6 - 8 = 16 \text{ ns}$$

enter these values into the MTBF equation

$$MTBF = \exp(t_d/k_2) / (k_1 * f_{CLK} * f_{DATA}) = 1.7 \times 10^{31} \text{ years}$$

To determine the maximum clock rate (e.g. $f_{CLK} = 1/(t_{SU} + t_d)$) that a device will allow in an asynchronous environment for expected MTBF, the following equation then can be used:

$$MTBF = \exp((1/f_{CLK} - t_{SU})/k_2) / (k_1 * f_{CLK} * f_{DATA})$$

Solving the equation for a 25 MHz data stream and 10 years MTBF expected for PEEL22CV10A-10, get the maximum clock rate $f_{CLK} = 52 \text{ MHz}$ and $t_{MET} = 5 \text{ ns}$.

Synchronizer Circuit Improves MTBF

Although PEELs show extremely quick metastable settling time, we still can improve the MTBF by using its unique internal feedback configuration. In Figure 4, a gated-latch internally latches the asynchronous input on the falling edge of the system clock, generating the signal Q1. ANDing the input with Q1 through the

internal feedback path eliminates a possible hazard condition during the clock's high-to-low transition time. The latch then holds Q1 stable to ensure meeting the setup-time requirement of the subsequent D flip-flop, which accepts data on the next rising system clock edge.

Just like a two stage synchronizer, the probability that a data goes metastable is the multiplication of the two probabilities of each synchronizer as they go metastable. Therefore since the probability of failure becomes so small, the MTBF of PEEL devices dramatically improves.

When using the same measurement setup above, we get $k_1 = 3 \times 10^{46}$ and $k_2 = 0.05 \text{ ns}$ for the same PEEL22CV10A-10 with a gated latch. With the same 25 MHz data rate and 10 years MTBF, the maximum clock frequency 70 MHz can be reached. As a result almost no extra delay is needed for the synchronizer.

References

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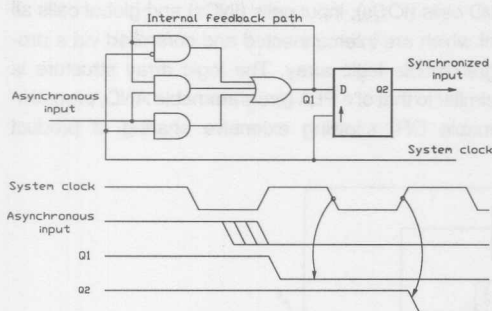


Figure 4. PEEL22CV10A Synchronizer

Ease Complex Waveform Generation with PEEL Arrays and ABEL

Introduction

Video, telecommunications, and other complex data transfer and control applications can often require waveform generation spread out over hundreds or thousands of clock cycles. Defining a PLD logic structure to generate such large sequences, with conditional variables, can at first glance be quite unwieldy. However, a straightforward method for generating long waveform sequences can be accomplished using a large counter which is decoded to generate and gate the necessary output signals. This method is similar to Mealy and Moore state machine structures but tailored for waveform generation by using a dedicated counter.

Although the concept is quite simple, finding the right PLD solution and an easy method for specifying the pattern is a bit more perplexing. Most PLDs provide the basic architecture for supporting small state machines and counters, but they often fall shy of resources when more complex and lengthy waveform sequences are needed.

Programmable Electrically Erasable Logic (PEEL) Arrays from ICT are a family of CPLDs in small pin count packages based on CMOS EEPROM technology. PEEL Arrays are ideal for waveform generation since they provide a logic intensive architecture with "I/O-buried" registers for counters, input latches for signal synchronization, and shared product terms that allow maximum utilization for count decoding. Specifying the

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waveform pattern can be done effectively using a combination of high level language techniques such as those provided by ABEL PLD Design Software from Data I/O.

PEEL Array Overview

The PEEL Array family includes three members: the PA7024, PA7128 and PA7140 in reprogrammable DIP, PLCC and SOIC packages ranging from 24 to 44 pins. The PEEL Array architecture is based on a versatile multi-level logic array architecture rich in latches, registers and sum-of-product functions. As illustrated in Figure 1, the main elements of the PEEL Array architecture include logic control cells (LCCs), I/O cells (I/OCs), input cells (INCs) and global cells all of which are interconnected and controlled via a programmable logic array. The logic array structure is similar to that of a PLA (programmable AND, programmable OR) allowing extensive sharing of product

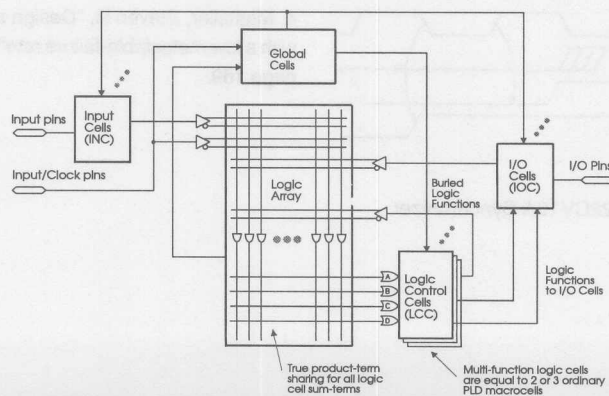


Figure 1. PEEL Array architecture

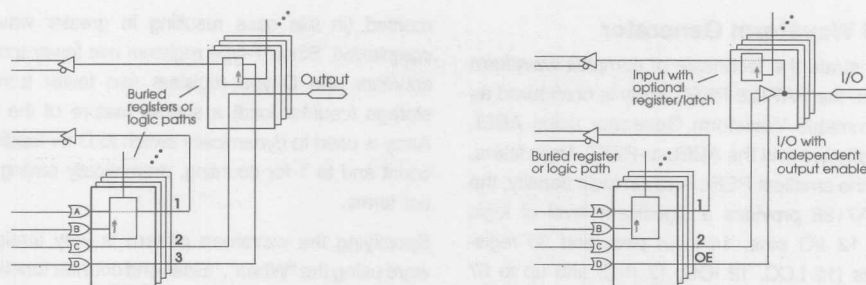


Figure 2: PEEL Arrays have multiple outputs per cell equal to 2-3 ordinary PLD macrocells. Thus, cell registers can be buried without limiting I/Os to input-only. Two possible Logic Cell and I/O cell configurations, with buried registers, are shown above.

terms. Logic resources among the three arrays range from 40-60 latches/registers and 40-72 complete sum-of-product logic functions, most of which can be buried. To put this into perspective, most 24-pin PLDs have only 8-10 registers and 8-10 sum-of-product logic functions, none of which can be buried.

PEEL Arrays offer the most flexible logic and I/O cells of any CPLD available today. Logic cells are user-configurable to implement multiple combinatorial and sequential functions based on four sum-of-product functions fed from the array. Logic cell registers can be D, T and JK type with independent or global clocks, resets, presets, clock polarity and other special features, all with full sum-of-products control. They also provide I/O cells with independent output enables. Possibly the most important feature of the logic cell is its ability to have multiple outputs making each logic cell equivalent to two or three ordinary PLD macrocells. This feature allows registers and combinatorial logic to be buried without limiting the use of I/O pins to input-only as other CPLDs do. See Figure 2.

ICT's CMOS EE technology offers high-speed performance with wide-gate delays as fast as 9ns for internal (buried) logic and 15ns external (pin to pin) logic. PEEL Array clock frequencies can be as fast as 80MHz for sequential functions such as counters and state machines.

Besides waveform generation, PEEL Arrays are ideal for implementing a wide variety of general purpose combinatorial, synchronous and asynchronous logic applications. Additionally, since PEEL Arrays allow for multi-level buried logic, designs normally requiring multiple PLDs and/or random logic can be efficiently integrated.

Development support for PEEL Arrays is provided by ICT and popular third party development tool and programmer manufacturers. ICT offers the powerful PLACE Development Software (free to qualified PLD designers) complete with architectural editor, logic compiler, and waveform simulator. Development with ABEL and CUPL is accommodated by PEEL Array fitters from ICT.

ABEL-to-PEEL Fitter

The ABEL-to-PEEL Fitter creates programming files for ICT's PEEL Array family using ABEL. The ABEL development methodology is fully maintained through design entry, compilation and functional simulation. The fitter operates on the "Berkeley Espresso" PLA files produced by ABEL, and creates PEEL Array JEDEC programming files.

ABEL-to-PEEL provides true device independent design entry, thus it is not necessary to specify pin numbers, node numbers, or global clock, reset and preset nodes. The fitter automatically optimizes the placement of logic cells and I/Os for the best fit and stores the resulting configuration in a ".log" file for review. Such device independent entry eases retargeting a design from one device to another.

The fitter can optionally create an ICT ".psf" (PLACE source file) allowing ABEL users to view the architectural configuration of the PEEL Array using the PLACE editor. It also allows the PLACE compiler or waveform simulator to be used in addition to ABEL. The ABEL-to-PEEL Fitter operates on PC compatibles with DOS 5.0 or greater and Sun SPARCstations with Sun OS 4.0.3 or greater.

PA7128 Waveform Generator

To demonstrate the technique of complex waveform generation, the PA7128 PEEL Array is configured as a Programmable Waveform Generator using ABEL Design Software and the ABEL-to-PEEL Array fitters. Although the smallest PEEL Array in logic density, the 28-pin PA7128 provides a significant level of logic including 12 I/O pins, 14 input pins, and 36 registers/latches (12 LCC, 12 IOC, 12 INC) and up to 67 product terms which can be shared by any logic function.

A block diagram of a Programmable Waveform Generator design is illustrated in Figure 3. The design consists of a buried 12-bit loadable counter, an 8-bit latch, an 8-bit comparator, input synchronization latches, waveform decode logic, and microprocessor interface, all in a cost effective 28-pin package. The processor interface allows a "first count" value to be written to the counter, as well as "last" value to the latch. The counter will start counting after it is written and will continue to count until it reaches the last count as detected by the comparator. The waveform outputs (W0-W10) are generated by decoding the state of the counter (Q0-11). The decode logic can also be used to gate input signals into the waveform pattern. When the last count is reached, the Done output is asserted as an interrupt to the processor to indicate that a new pattern can be generated. The 12-bit counter, with upper 8-bits loadable, can accommodate a single sequence that is 4096 clocks long or as many as 256 sequences that are 16 clocks long.

Because PEEL Array logic functions share product terms, minimizing terms allow more logic to be imple-

mented (in this case resulting in greater waveform complexity). Since T-type registers use fewer terms for counters and D-type registers use fewer terms for storage (counter load) a special feature of the PEEL Array is used to dynamically switch to D for loading the count and to T for counting, dramatically saving product terms.

Specifying the waveform pattern is very straightforward using the "When", "Else" and counter functions of the ABEL design software. Figure 4 shows a partial listing of the equations necessary to generate three sets of waveform patterns over 4096 clocks. The patterns also allow gating of input signals that are synchronized via the PA7128's input registers.

Since waveforms are decoded via product terms, there is a finite limit to the complexity of patterns. However, by using various ABEL logic reduction algorithms and specifying event changes on even binary boundaries, the number of events can be maximized. This implementation uses eleven outputs and is best suited for short repetitive patterns over long count ranges. If greater complexity is needed then fewer outputs should be used which will free up product terms for additional events. Complexity can also be increased by using a PEEL Array with greater logic density, such as the PA7024 or PA7140.

Although this application example used a single long counter, the technique is also applicable for smaller counters with decoding logic. In fact, PEEL Array architectures provide multiple clock sources per register, allowing several independent counters with waveform decoding to be implemented within a single device.

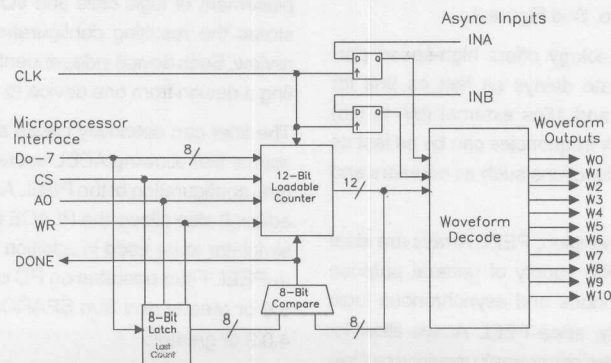


Figure 3. Programmable Waveform Generator implemented in ICT's 28-pin PA7128

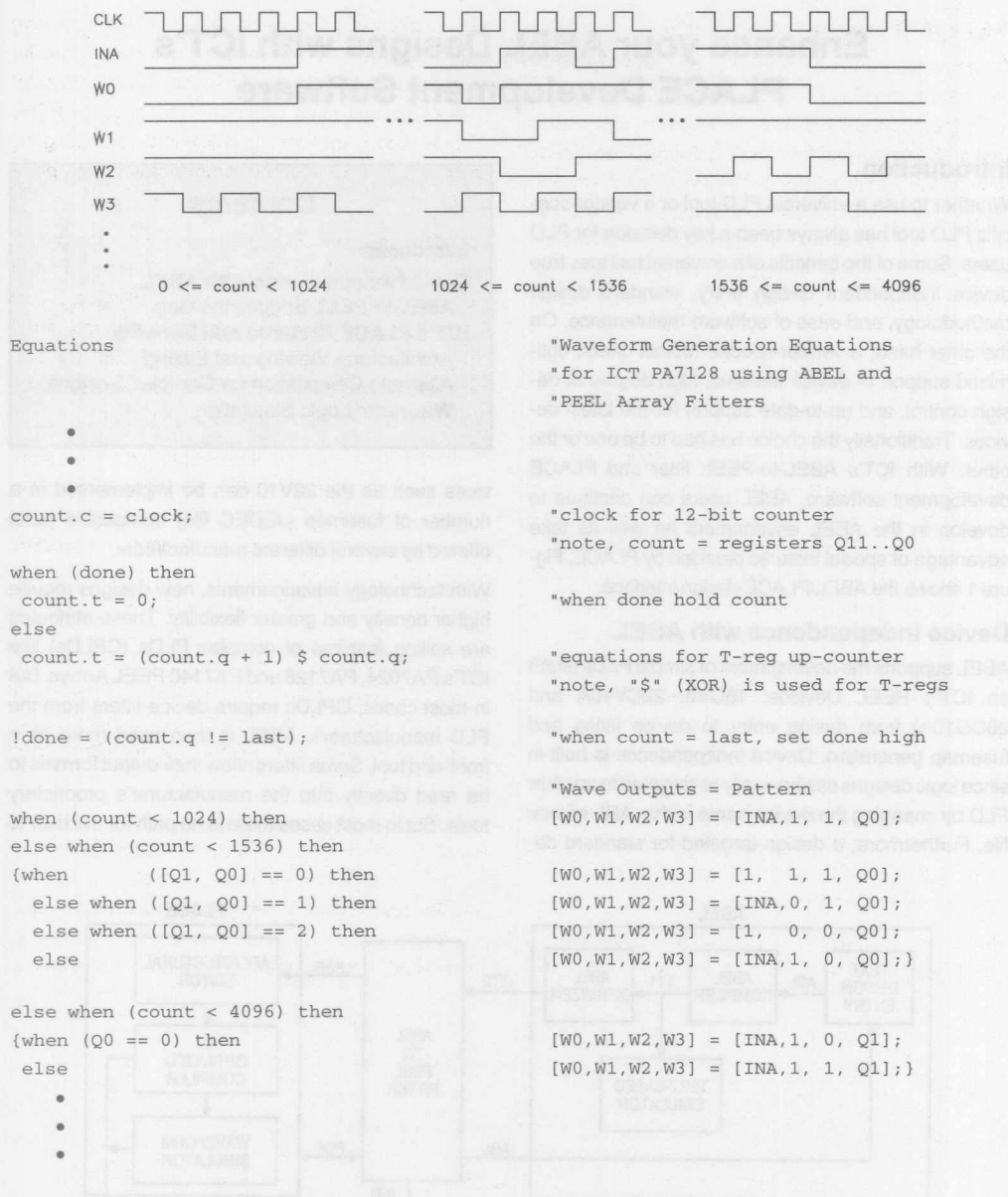


Figure 4: ABEL source equations and resulting waveforms for PA7128 waveform generator

Enhance your ABEL Designs with ICT's PLACE Development Software

Introduction

Whether to use a universal PLD tool or a vendor-specific PLD tool has always been a key decision for PLD users. Some of the benefits of a universal tool are: true device independent design entry, standard design methodology, and ease of software maintenance. On the other hand, a vendor-specific toolset offers: optimized support of device features, high degree of design control, and up-to-date support for the latest devices. Traditionally the choice has had to be one or the other. With ICT's ABEL-to-PEEL fitter and PLACE development software, ABEL users can continue to develop in the ABEL environment as well as take advantage of special features provided by PLACE. Figure 1 shows the ABEL/PLACE design interface.

Device Independence with ABEL

ABEL supports the development of simple PLDs (such as ICT's PEEL Devices: 18CV8, 22CV10A and 20CG10A) from design entry to device fitting and fusemap generation. Device independence is built-in since logic designs can be easily re-targeted to another PLD by changing the device name in the .ABL source file. Furthermore, a design targeted for standard de-

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Architectural Viewing and Editing

Alternate Compilation for Complex Designs

Waveform Logic Simulation

vices such as the 22V10 can be implemented in a number of fusemap (JEDEC file) compatible parts offered by several different manufacturers.

With technology advancements, new designs require higher density and greater flexibility. These attributes are selling features of complex PLDs (CPLDs) like ICT's PA7024, PA7128 and PA7140 PEEL Arrays. But in most cases, CPLDs require device fitters from the PLD manufacturers. ABEL is then used more as a front-end tool. Some fitters allow their output formats to be read directly into the manufacturer's proprietary tools. But in most cases there is no path for the user to

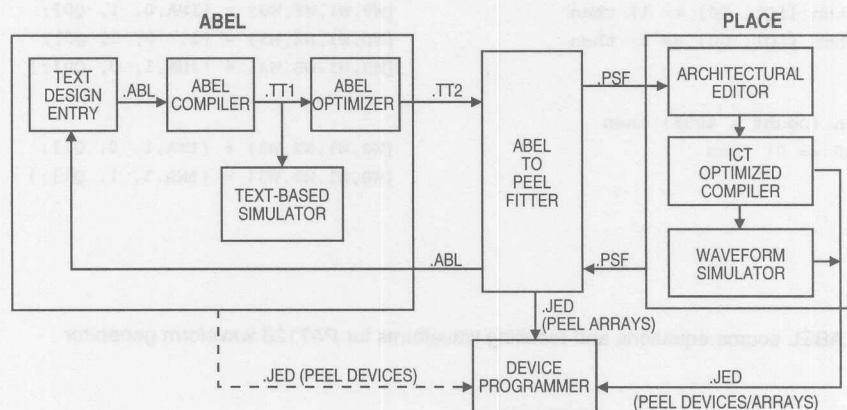


Figure 1. ABEL/PLACE Design Interface

back-annotate the design changes to the ABEL source file. The alternative is to make the changes in the original ABEL source file and re-compile it through the device fitter.

ABEL-to-PEEL Bridges the Gap

ICT's ABEL-to-PEEL fitter provides a two-way bridge between the standard ABEL environment and ICT's powerful and easy-to-use PLACE software for PC-based systems. The fitter interfaces with ABEL using the PLA format and executes under the SmartPart module. A PLACE source file (PSF) may be generated for a fitted PEEL Array design. The ABEL-to-PEEL fitter can convert a PSF for any PEEL Array CPLD back to an ABEL source file.

ICT's PLACE Features and Benefits

ICT's PLACE development software provides a graphical user interface for design entry, logic compilation, design simulation, and device programming.

The benefits of the PLACE software to ABEL users are:

1. Architectural Viewing and Editing
2. Alternate Compilation for Complex Designs
3. Waveform Logic Simulation

Architectural Viewing and Editing

The PLACE software reads the PSF output from the ABEL-to-PEEL fitter and displays the architectural details of a fitted design. Figure 2 (next page) shows the PLACE architectural editor displaying the block diagram of a PA7140 design.

Inside the PLACE architectural editor, device architectural features are edited graphically. For example, with

the click of a mouse button, a D-type flip-flop can be switched to a T-type or the clock source can be changed from the global line to the output of a sum-term. Figure 3 shows the architectural details of Logic Control Cell 4A and I/O Cell 9 of the PA7140 design. This feature is especially beneficial for new users learning the architectural capability of the devices. It also allows advanced CPLD designers to get the greatest possible utilization of the parts.

Alternate Compilation for Complex Designs

The ABEL optimizer can perform logic reduction by "pin" for programmable-AND, fixed-OR architectures (such as the PEEL22CV10A) or by "group" for basic programmable-AND, programmable-OR PLA architectures. However, it has difficulty achieving the best possible optimization for PLA architectures like PEEL Arrays that provide complete "sum-of-products" logic functions for clocks, presets and resets. Thus when complex designs do not fit using the ABEL fitter, the PLACE compiler can be used for a more extensive group-level logic reduction with optimized positive and negative polarities for all logic functions. In fact, the PLACE compiler offers five levels of logic reduction and minimization control.

Waveform Logic Simulation

The PLACE simulator allows test vectors to be edited and displayed graphically. The multi-level simulator uses a color and line-style scheme to show external signals, internal nodes, inputs and outputs. The logic analyzer-like waveform display make design verification easy and intuitive. Figure 4 shows the waveform simulation screen in PLACE.

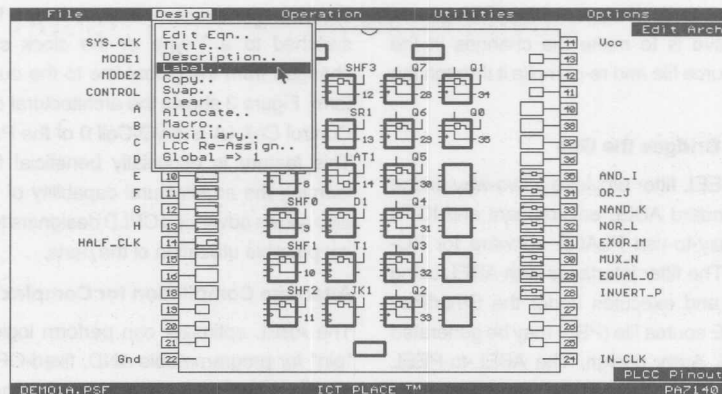


Figure 2. PLACE Architectural Editor

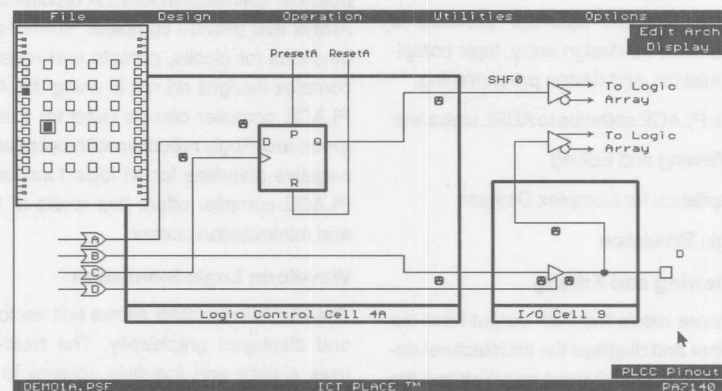


Figure 3. PLACE Architectural Details of a Logic Cell

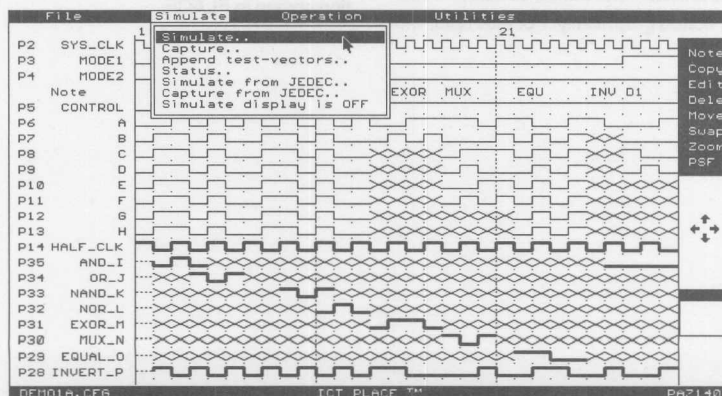


Figure 4. PLACE Waveform Simulation

PEEL™ Device Characterization Report

Introduction

The following data provides typical and worst case measurements for several key AC and DC parameters for 1.0 micron PEEL16V8, 18CV8, 20CG10A and 22CV10A products. Normalized characterization graphs are included. Data for 0.8 micron PEEL Devices such as the PEEL22CV10A-5, 20CG10A-5, PEEL20V8 and 22CV8 is similar.

DC Characterization Data

Supply Current vs Ambient Temperature and Vcc

The effects of power supply current (Icc) vs Vcc voltage and ambient temperature are provided on normalized graphs. Typical Icc measurements may be used in

Product	Icc (mA)	
	Typical	Maximum
18CV8-5	65	90
18CV8-7	75	110
18CV8-10	65	110
18CV8-15	28	45
18CV8-25	18	37
22CV10A/20CG10A-5	95	140
22CV10A/20CG10A-7	100	155
22CV10A/20CG10A-10	80	135
22CV10A/20CG10A-15	70	135
22CV10AL/20CG10AL-15	55	75
22CV10A/20CG10A-25	40	67

Note: Typical ICC at Temp=25°C, Vcc=5.0V, Freq=25MHz;
Maximum at Temp=0-70°C, Vcc=5.25V, Freq=25MHz. See the respective data sheets for Icc typical and maximum values for the PEEL16V8, PEEL20V8, and PEEL22CV8.

Table 1. Characterization Data

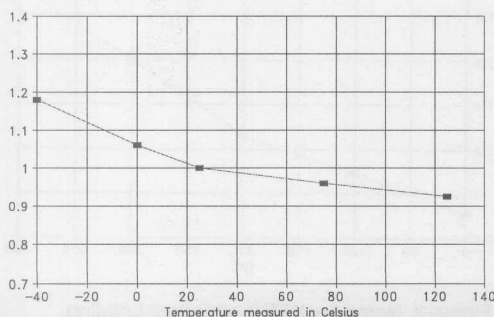


Figure 1a. Normalized ICC vs Temperature

Contents

Introduction

DC Characterization Data

- Supply Current vs Temperature and Vcc
- Package Thermal Characteristics
- Output Sink/Source Current vs Output Voltage

AC Characterization Data

- Speed vs Capacitive output Loading
- Output Slew Rates and Ground Bounce
- Speed vs Temperature and Vcc

conjunction with the normalized graphs to ascertain additional data concerning variations over temperature or Vcc. Figure 1a shows variations in temperature at Vcc = 5.0V. Figure 1b shows variations in Vcc at Temperature = 25°C.

Package Thermal Characteristics

The PEEL Devices and PEEL Arrays are available in plastic DIP, plastic LCC and SOIC packages. Thermal characteristics of these packages are specified by the thermal (junction to ambient) resistance value "θJA". Used in conjunction with the PEEL Device's and PEEL Array's power dissipation and a reference operating temperature, the thermal resistance can determine junction temperature (T junction = T reference + Power × θJA). For example, the θJA for ICT's 24 pin plastic DIP package is approximately 60°C/Watt and the θJA for ICT's 28 pin plastic LCC (PLCC) package is approximately 58°C/Watt. Contact ICT for additional package thermal characteristics.

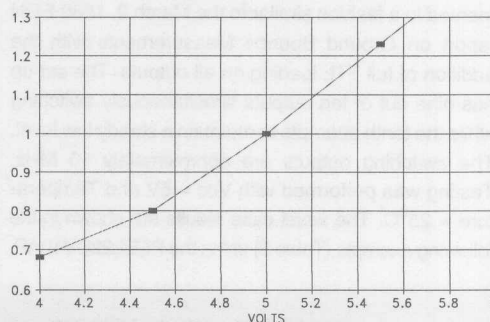


Figure 1b. Normalized ICC vs VCC

Output Sink and Source Current vs Output Voltage

Two graphs (Figures 2a and 2b) plotting the relative effects of output current vs voltage are provided: Output sink current (IOL) vs Output voltage low (VOL) and Output source current (IOH) versus Output voltage high (VOH). Data for both graphs use Vcc = 5.0V and Temperature = 25°C.

	Typical	Data Sheet Limit
IOL @ VOL .5V	32mA	16mA
VOL @ IOL 16mA	0.22V	0.5V
IOH @ VOL 2.4V	-33mA	-4mA
VOH @ IOL -4mA	3.8V	2.4V

Note: Typical measurement at Temp=25°C, Vcc=4.75V

Table 2. Output Drive

AC Characterization Data

Speed vs Capacitive Output Loading

The effects of capacitive output loading on Tpd are provided on a normalized graph in Figure 3. Typical Tpd measurements can be used in conjunction with the normalized graph to ascertain additional data concerning loading variations. All measurements were taken with Vcc = 5.0 and Temperature = 25°C.

Output Slew Rates and Ground Bounce

Output buffers of the PEEL devices have a nominal slew rate of 1V/ns for both low-to-high and high-to-low transmissions between 0 and 3V. The slew rate is fast enough to meet 22CV10A speed requirements but slow enough to minimize bounce and transmission line effects.

Ground bounce testing of the PEEL devices is implemented in a fashion similar to the March 2, 1989 EDN report on Ground Bounce Measurements with the addition of full TTL loading on all outputs. The set-up has nine out of ten outputs simultaneously switching while the tenth attempts to maintain a steady low level. The switching outputs are approximately 10 MHz. Testing was performed with Vcc = 5V and Temperature = 25°C. The worst case results are shown in the following example (Table 3) using the PEEL22CV10AP.

22CV10AP

9 Switched Outputs	Unswitched Outputs Voltage Peak (TTL load)
Low-High	0.42V
High-Low	0.83V

Table 3 Ground Bounce

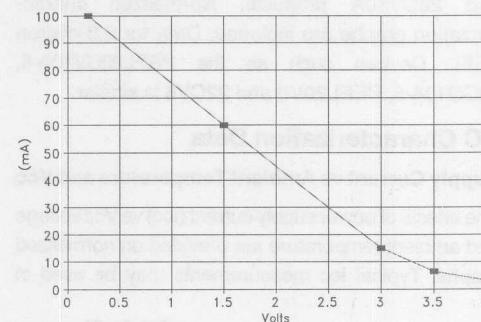


Figure 2a. IOH vs VOH

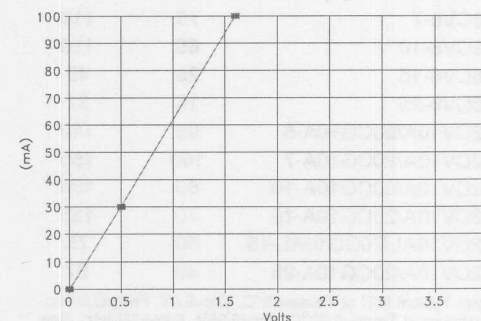


Figure 2b. IOL vs VOL

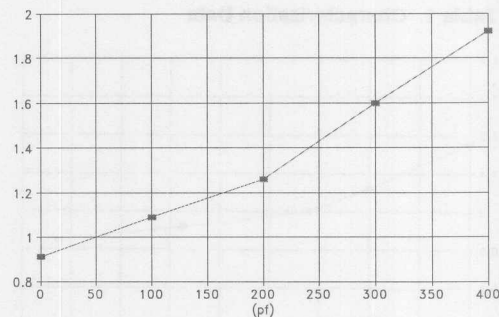


Figure 3. Normalized TPD vs Output Loading

Product	Tpd (ns)		Tco (ns)		Tsc (ns)	
	Typical	Maximum	Typical	Maximum	Typical	Maximum
18CV8-5	4.5	5	3.7	4	1.8	3.5
18CV8-7	5.5	7.5	5	7	3	5
18CV8-10	8	10	5	7	3.5	5
18CV8-15	12	15	8	12	8	12
18CV8-25	18	25	10	15	10	20
22CV10A/20CG10A-5	4.5	5	3.7	4	2	3
22CV10A/20CG10A-7	5.5	7.5	4	5.5	2.5	3
22CV10A/20CG10A-10	8	10	4.5	6	3.5	5
22CV10A/20CG10A-15	12	15	6	8	6	8
22CV10AL/20CG10AL-15	13	15	7	10	7	10
22CV10A/20CG10A-25	16	25	10	15	10	15

Note: Typical at Temp=25°C, Vcc=5.0V, Freq=25MHz; Maximum at Temp=0-70°C, Vcc=4.75-5.25V, Freq=25MHz. Contact ICT for typical data for components not listed in this table.

Table 4. Characterization Data

Speed Vs Temperature and Vcc

The effects of ambient temperature and Vcc voltage vs speed (Tpd, Tco and Tsc) are provided on normalized graphs in Figures 4a - 4f. The typical speed measurements shown in Table 4 may be used in conjunction with the normalized graphs to derive additional data

concerning variations over temperature or Vcc. Graphs showing variations in temperature use Vcc = 5.0V. Graphs showing variations in Vcc use Temperature = 25 degrees C. Standard data sheet test loads are used.

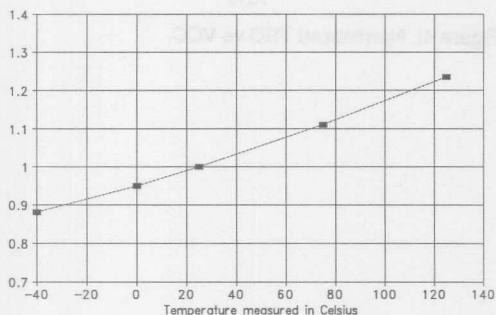


Figure 4a. Normalized TPD vs Temperature

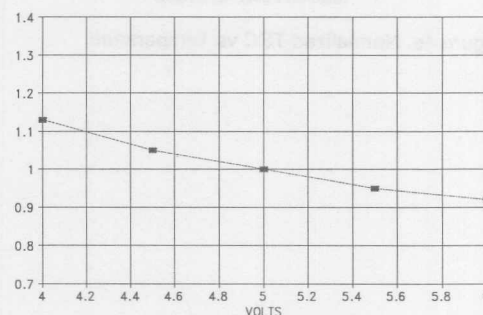


Figure 4b. Normalized TPD vs VCC

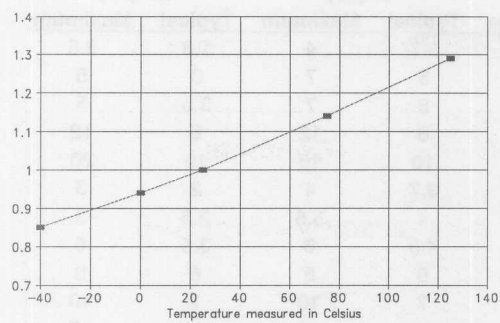


Figure 4c. Normalized TCO vs Temperature

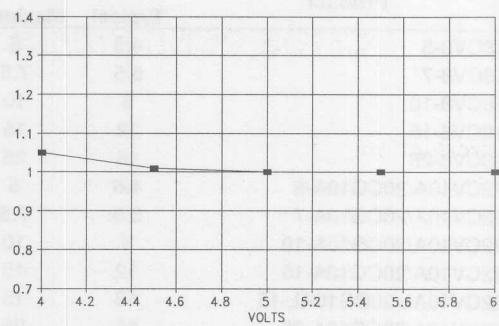


Figure 4d. Normalized TCO vs VCC

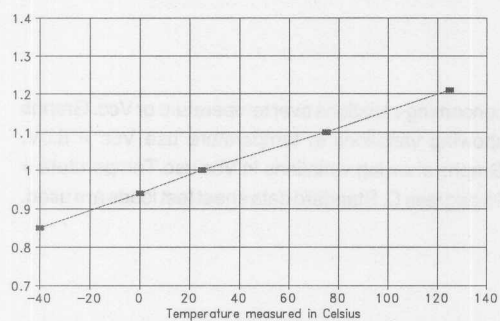


Figure 4e. Normalized TSC vs Temperature

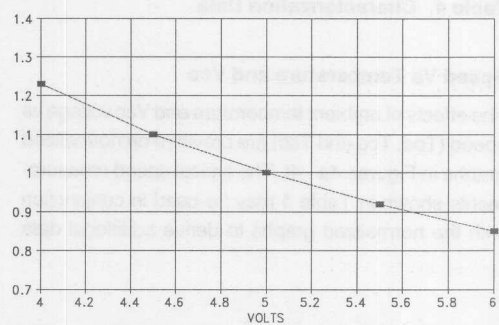


Figure 4f. Normalized TSC vs VCC

CMOS PEEL Products Reliability Report

Introduction

ICT Inc. is dedicated to providing its customers with integrated circuits that are designed, manufactured, tested and serviced to the highest level of Quality and Reliability. This reliability report provides a summary of ICT's CMOS EEPROM process for PEEL devices and Arrays. It also documents the reliability tests performed and the data collected to ensure our reliability and quality standards. Additionally, an overview of ICT's standard production test flow is included.

CMOS EEPROM Process Overview

ICT's 0.8 μ m and 1.0 μ m processes are N-well based CMOS processes. The N-well approach is chosen for optimal low power consumption while balancing the performance of both N-Channel transistors and memory cells. Two layers of polysilicon for the memory cell allows the first poly layer to be used as the floating gate, while the second poly layer is used for the control gate and peripheral transistor gate.

The transistors have a high quality gate oxide, with 0.8 μ m effective channel length. The EEPROM memory cell has 100 Å tunnel oxide between the floating gate and the drain side. Charge injection into and out from the floating gate are accomplished by the Fowler Nordheim tunneling mechanism. This process utilizes double metal layers to minimize the signal delay time and reduce chip size. High breakdown voltages are achieved by a graded drain/source junction.

To simplify the design and processing steps ICT's EEPROM technology, unlike that of other EEPROM manufacturers, does not require EPI materials or substrate bias generators. This reduces the number of mask steps, improving reliability and yield. High CMOS latchup immunity and High ESD protection are achieved by a double guard band design in the chip layout.

Reliability Tests

Reliability test for ICT's initial device qualification include: operating life, data retention, endurance, temperature cycling, pressure pot, temperature humidity bias stress, latch-up and electro-static discharge

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Introduction

CMOS EEPROM Process Overview

Reliability Tests

Operating Life
Data Retention
Endurance
Temperature Cycling
Pressure Pot
Temperature Humidity Bias Stress
Latch-up
Electro-static discharge (ESD)

6

(ESD). Reliability related tests, such as data retention, are also incorporated into ICT's standard production test flow.

After initial device qualification, all products are carefully monitored to ensure the reliability of the device. Production lots are periodically sampled, and are subject to the same qualification tests; all results are documented and failures are carefully analyzed in order to make long term improvements to the product.

PEEL Devices and Arrays developed with ICT's CMOS EEPROM processes share extensive design commonality and more significantly, they share the same memory cell structure. Furthermore, these devices are manufactured using similar molding compounds, test flows, and advanced screening techniques. These similarities make the reliability data of each device relevant to the others.

Test data provided in this report is applicable to the following PEEL Device and PEEL Array products:

PEEL16V8	PA7024
PEEL18CV8	PA7128
PEEL20V8	PA7140
PEEL22CV8	
PEEL20CG10A	
PEEL22CV10A	
PEEL22CV10AZ	

Device	Lot #	168 hrs	500 hrs	1000 hrs	Failure Mode
18CV8	ICTM05032	0/105	0/105	0/105	
18CV8	CTM24063	0/105	0/105	0/105	
18CV8	CTM24166	0/105	0/105	0/105	
18CV8	CTM29186	0/105	0/105	0/105	
18CV8	CTM32602M	0/105	0/105	0/105	
18CV8	CTM32004M	0/105	0/105	0/105	
18CV8	CTM46013	0/105	0/105	0/105	
18CV8	CTM36087	0/105	0/105	0/105	
18CV8	CTM51908V	0/105	0/105	0/105	
18CV8	CTM39001	0/105	0/105	0/105	
18CV8	CTN08618V	0/105	0/105	0/105	
18CV8	7980	0/105	0/105	0/105	
18CV8	CTN46608AG	0/105	0/105	0/105	
22CV8*	CTN18638	0/105	0/105	0/105	
22CV10A	TL27075	0/105	0/105	0/105	
22CV10A	CTM29188	0/105	1/105	0/104	Single I/O pin
22CV10A	9738	0/105	0/105	0/105	
22CV10A	7938	0/105	0/105	0/105	
22CV10A	CTM22037M	0/105	0/105	0/105	
22CV10A	CTM42152F	0/105	0/105	0/105	
22CV10A	CTM41175F	0/105	0/105	0/105	
22CV10A	CTM46217F	0/105	0/105	0/105	
22CV10A	7979	0/105	0/105	0/105	
22CV10A	CTM34031	0/105	0/105	0/105	
22CV10A	CTN25615	0/105	0/105	0/105	
22CV10A	TL37075	0/105	0/105	0/105	
22CV10A*	TL38110	0/105	0/105	0/105	
PA7024	TL10058	1/105	0/104	0/104	Single I/O pin
PA7024	TL11059	0/105	0/105	0/105	
PA7024	TL16020	0/105	0/105	0/105	
PA7024	CTM31016HA	0/105	0/105	0/105	
PA7024	CTM31089HA	0/105	0/105	0/105	
PA7024	CTM34042HA	0/105	0/105	0/105	
PA7128	ICTM08138E	0/105	0/105	0/105	
PA7128	CTM42030	0/105	0/105	0/105	
PA7128	CTM45004	0/105	0/105	0/105	
PA7140	CTM42030	0/105	0/105	0/105	
Total		1/3885	1/3884	0/3883	

Continuous operation, Bias voltage=5.25V, amb. temp=125°C, duration=1000 hours. *These are 0.8µm, all others are 1.0µm.

Table 1. Dynamic High-Temperature Operating Life Test Data

Device Hrs @ 125°C	Activation Energy	Equivalent Hrs at:		# of Failures	Predicted Fail Rate at:	
3,883,668	1.0eV	70°C	55°C	2	70°C	55°C
		4.2E8	2.0E9		8 FITS	2 FITS

ICT takes a conservative approach to calculate FIT rates. Three failures are assumed for worst case calculations.

Table 2. Failure Rate Predictions at 60 % U.C.L.

Operating Life

Dynamic High-Temperature Operating Life (DHTOL) test is a standard approach used to evaluate the reliability of a product under accelerated conditions. Data is gathered at the rated ambient temperature and the devices are biased as they would be in actual operation. The devices are exercised by constantly switching the inputs.

The results of the DHTOL test are recorded in a datalog and made available for future reference, see Table 1. Failure rates in this reliability report are expressed in FITS. Since integrated circuits exhibit very low failure rates, it is convenient to refer to failures in a population during a period of 10^9 devices hours; one failure in 10^9 device hours is defined as one FIT, see Table 2.

Data Retention

At the cell level, data retention is a function of the floating gate's ability to retain charge over extended periods of time without an applied gate bias. Data retention failures in a floating gate structure are commonly caused by dielectric defects which cause undesired leakage paths; these failures can be accelerated by high-temperature bake stress. The purpose of this test is to determine the reliability of the floating gate's ability to retain charge beyond the normal 10 years of operation. Production devices are subjected to a non-biased bake of 165°C with a duration of 57 hours for commercial and 228 hours for industrial. See Table 3.

Endurance

An ICT EEPROM endurance specification means that for any lot of devices shipped, fewer than 5% of the units will cease to cycle properly before the specified limit. Endurance refers to the maximum number of erase and write operations through which each memory cell can be reliably cycled. Standard specified limits

for both PEEL Devices and PEEL Arrays are 1,000 cycles. However, due to the highly reliable 100 Å tunnel oxide, the actual endurance characteristics are typically significantly better. ICT incorporates into the standard production test flow, a proprietary endurance procedure that allows monitoring of endurance characteristics to specifications.

Temperature Cycling Air to Air

The device is cycled at temperature extremes in a nitrogen environment without power. The normal temperature extremes are -65°C to $+150^{\circ}\text{C}$ with a minimum dwell time of 10 minutes at each of the temperatures and 5 minutes transfer time according to mil STD 883C method 1010.5 condition C. This test measures die stress to the mechanical condition of the package because the thermal coefficient of die are not the same as those of the encapsulation mold compound or the leadframe. See Tables 4a and 4b.

Pressure Pot

The device is exposed to saturated steam at high temperature and pressure. The normal condition is 20 PSI at 127°C . The corrosion resistance of the die in a moist ambient is a key package reliability issue. The plastic encapsulate is not a moisture barrier and will saturate within 72 hours. Since the die is not powered, its temperature and relative humidity will be the same as autoclave once equilibrium is reached. The environmental conditions are now such that it has an ample supply of steam and temperature to start thermally activated events. Autoclave is a good test to detect cracks and holes in the encapsulating plastic and contamination induced leakage problems inadvertently added during the assembly operation. See Table 5.

Temperature Humidity Bias Stress

This accelerated temperature and humidity bias stress is normally performed at 85°C and 85% relative humid-

Device	Lot #	57 Hrs.	168 Hrs.	336 Hrs.	500 hrs.	Failure Mode
18CV8	TL38109	0/210	0/210	0/210	0/210	
18CV8	TL41139	0/210	0/210	0/210	0/210	
18CV8	TL41140	1/210	0/209	0/209	0/209	Bit Failure
22CV10A	TL25052	0/210	0/210	0/210	0/210	
22CV10A	TL21110	0/210	0/210	0/210	0/210	
Total Hours = 524,500						

Using activation energy of 1.0 eV, 500 hours at 165°C is equivalent to 87.7 years at 70°C or 420 years at 55°C of data retention on floating gate.

Table 3. Data Retention

ity. To maximize metal corrosion conditions, the worst-case bias is the one which has least power dissipation and maximum voltage applied. Higher power dissipation tends to lower humidity at the chip surface and hence lower corrosion susceptibility. This test was performed with alternate pins biased to +5 volts or 0 volts. See Table 6.

Latch-Up

To prevent latch-up a double guard-ring is used on all I/O pins of PEEL Devices and PEEL Arrays. The double guard-ring consists of a dummy N-well ring

around the P transistor and a P+ ring around the N transistor.

Positive bias latch-up: Positive bias latch-up tests are performed to ensure reliability for positive bias of up to +16V. Above +16V, gate assisted breakdown may occur destroying the device.

Negative bias latch-up: Negative bias latch-up tests are performed to ensure reliability up to 100mA negative bias latch-up current ($V_{cc}=5V$, $V_{ss}=0$).

Device	Lot #	100 Cycles	500 Cycles	1000 Cycles
22CV10A	TL10042	0/30	0/30	0/30
22CV10A	TL11056	0/30	0/30	0/30
22CV10A	TL11057	0/30	0/30	0/30

MIL STD 883C Condition B (-55°C to 125°C)

Table 4a. Temperature Cycling Air To Air (-55°C to 125°C)

Device	Lot #	100 Cycles	500 Cycles	1000 Cycles
22CV10A	TL10042	0/30	0/30	0/30
22CV10A	TL11056	0/30	0/30	0/30
22CV10A	TL11057	0/30	0/30	0/30
18CV8	TL41139	0/105	0/105	0/105
18CV8	TL41140	0/105	0/105	0/105
18CV8	TL41141	0/105	0/105	0/105

MIL STD 883C Condition C (-65°C to 150°C)

Table 4b. Temperature Cycling Air To Air (-65°C to 150°C)

Device	Lot #	72hrs	168hrs.
22CV10A	TL10042	0/100	0/100
22CV10A	TL11057	0/100	0/100
18CV8	TL41139	0/105	0/105
18CV8	TL41140	0/105	0/105
18CV8	TL41141	0/105	0/105

Saturated steam @ 127°C, 20 PSIG

Table 5. Pressure pot

Device	Lot #	100 Hrs.	500 Hrs.	1000 Hrs.
18CV8	TL41138	0/105	0/105	0/105
18CV8	TL41140	0/105	0/105	0/105
18CV8	TL41141	0/105	0/105	0/105

MIL STD 883C Condition C (-65°C to 150°C)

Table 6. Temperature Humidity Bias Stress

Electro-static Discharge (ESD)

Electrostatic discharge (ESD) is evaluated per MIL-STD-883 Method 3015. The procedure implements a destructive test in which device pins are subjected to multiple ESD pulses at progressively increased voltages. Leakage current is monitored until a leakage current of greater than 1 μ A is measured at the pin. Electrostatic Discharge (ESD) testing on PEEL Devices and PEEL Arrays shows that all pins can withstand greater than 2000V.

Production Test Flow

ICT has developed a test flow to ensure that all products shipped to customers are of the highest quality and reliability. Each device is erased, programmed, and read at Wafer Sort, Package Test, and QA Test to guarantee electrical characteristics over the entire operating temperature range and functionality of the part. Test programs are developed to screen out those devices which fail to meet data sheet specifications.

Rather than relying exclusively on lot-sample-based reliability data, ICT has also incorporated 100% data retention verification into its standard production test flow. The test programs are developed to screen out those devices which fail to meet data sheet specifications. This is accomplished by subjecting all devices to a wafer-level data retention bake which verifies the ability to retain data for at least ten years over the entire temperature range (0 to 70°C for Commercial and -40 to 85°C for Industrial).

Figure 1 shows the general test flow for ICT's CMOS EEPROM-based product.

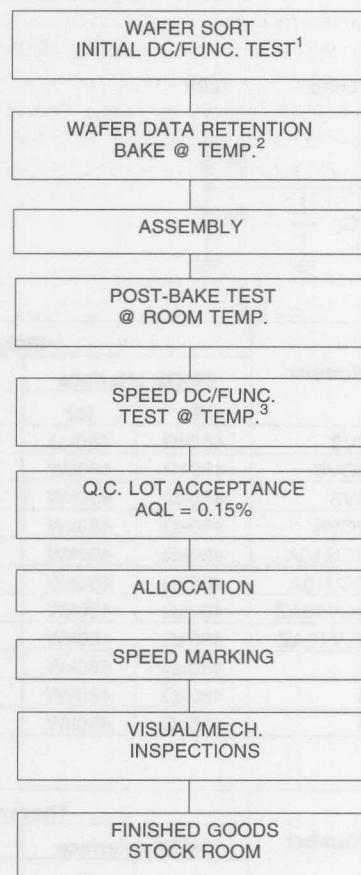
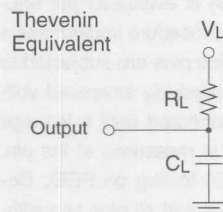
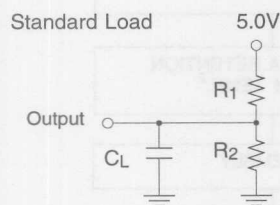


Figure 1. Test Flow for ICT PEEL Products

Notes :

1. All functional and parametric parameters are tested at room temperature. Proper Program/Verify operation is tested via multiple erase, write and read tests.
2. A proprietary procedure determines the time and temperature of the Data Retention Bake which verifies that the device will hold data for greater than ten years of operation at the maximum rated operation temperature.
3. Devices are tested at data sheet specifications.
Commercial Temp. = 0°C to 70°C
Industrial Temp. = -40°C to 85°C

PEEL Device and Array Test Loads



Part Number	Standard Loads				
	CMOS Interface		TTL Interface		CL
	R1	R2	R1	R2	
PEEL16V8	480kΩ	480kΩ	235W	159Ω	50pF
PEEL18CV8	480kΩ	480kW	235Ω	159W	50pF
PEEL20V8	480kΩ	480kW	235Ω	159W	50pF
PEEL22CV8	480kΩ	480kW	235Ω	159W	50pF
PEEL20CG10A	480kΩ	480kW	235Ω	159W	50pF
PEEL22CV10A	480kΩ	480kW	235Ω	159W	50pF
PEEL22CV10AZ	480kΩ	480kW	235Ω	159W	50pF
PEEL22LV10AZ	480kΩ	480kW	235Ω	159W	50pF
PA7024	480kΩ	480kW	235Ω	159W	50pF
PA7128	480kΩ	480kW	235Ω	159W	50pF
PA7140	480kΩ	480kW	235Ω	159W	50pF

Part Number	Thevenin Equivalent				
	CMOS Interface		TTL Interface		CL
	RL	VL	RL	VL	
PEEL16V8	228kΩ	2.375V	95Ω	2.02V	50pF
PEEL18CV8	228kΩ	2.375V	95W	2.02V	50pF
PEEL20V8	228kΩ	2.375V	95W	2.02V	50pF
PEEL22CV8	228kΩ	2.375V	95W	2.02V	50pF
PEEL20CG10A	228kΩ	2.375V	95W	2.02V	50pF
PEEL22CV10A	228kΩ	2.375V	95W	2.02V	50pF
PEEL22CV10AZ	228kΩ	2.375V	95W	2.02V	50pF
PEEL22LV10AZ	228kΩ	2.375V	95W	2.02V	50pF
PA7024	228kΩ	2.375V	95W	2.02V	50pF
PA7128	228kΩ	2.375V	95W	2.02V	50pF
PA7140	228kΩ	2.375V	95W	2.02V	50pF

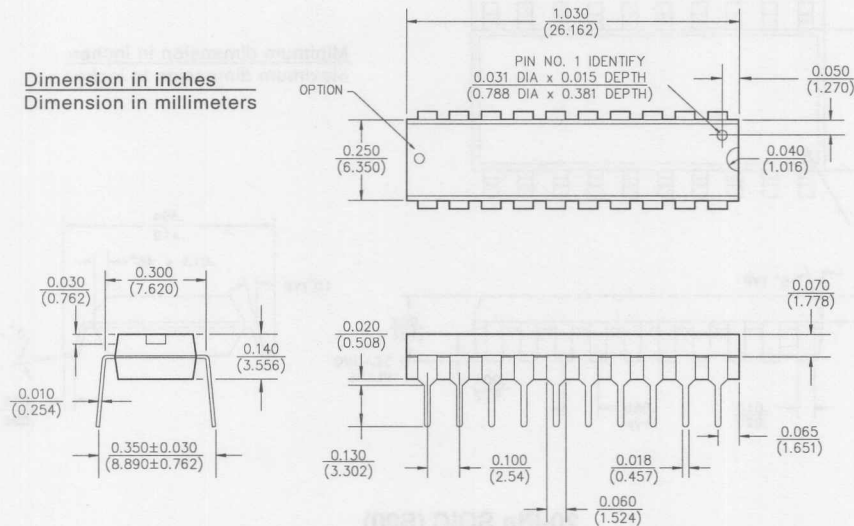
Package Information

7

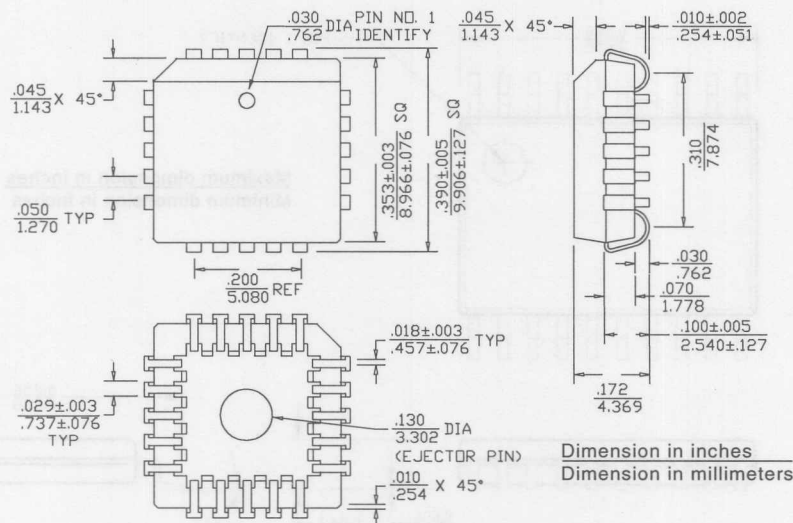
Package Diagrams 7-3

Package Diagrams (Drawings are not necessarily to scale.)

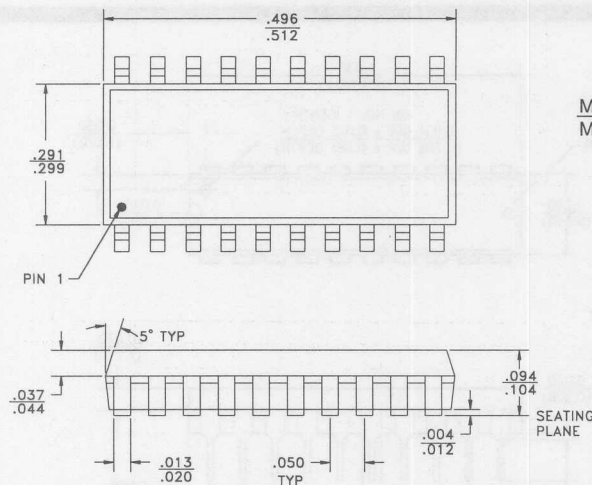
Dimension in inches
Dimension in millimeters



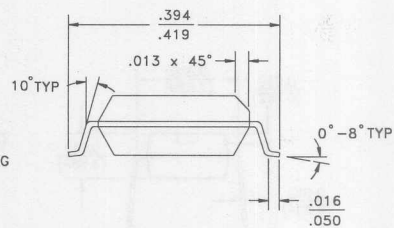
20-Pin Plastic DIP (P20)



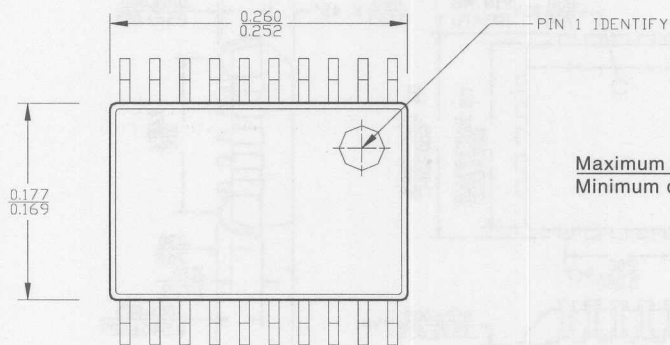
20-Pin PLCC (J20)



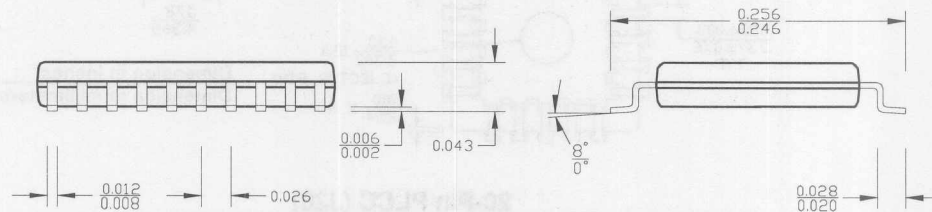
Minimum dimension in inches
Maximum dimension in inches



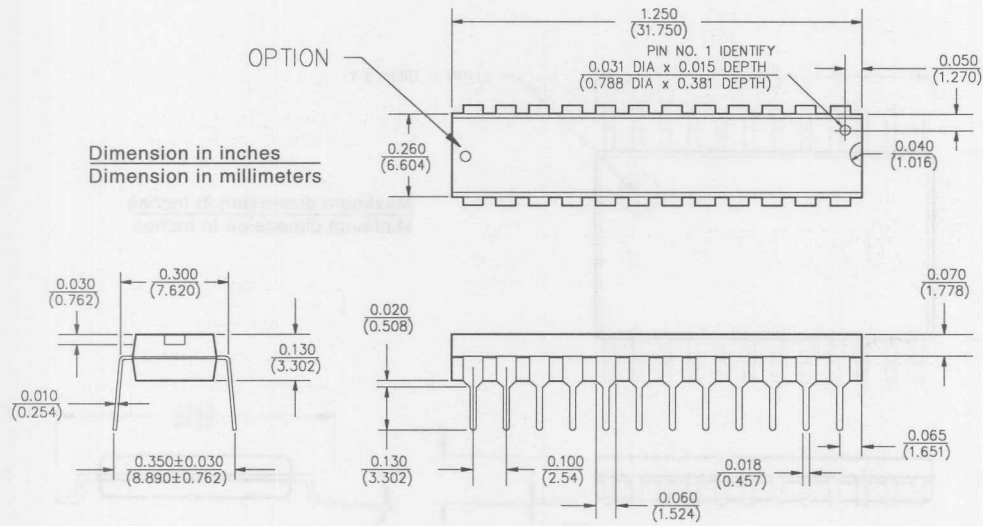
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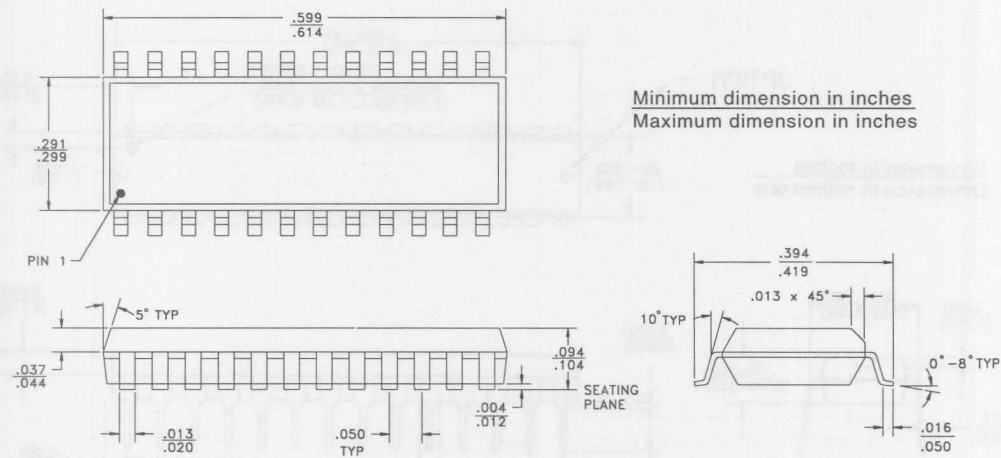
Maximum dimension in inches
Minimum dimension in inches



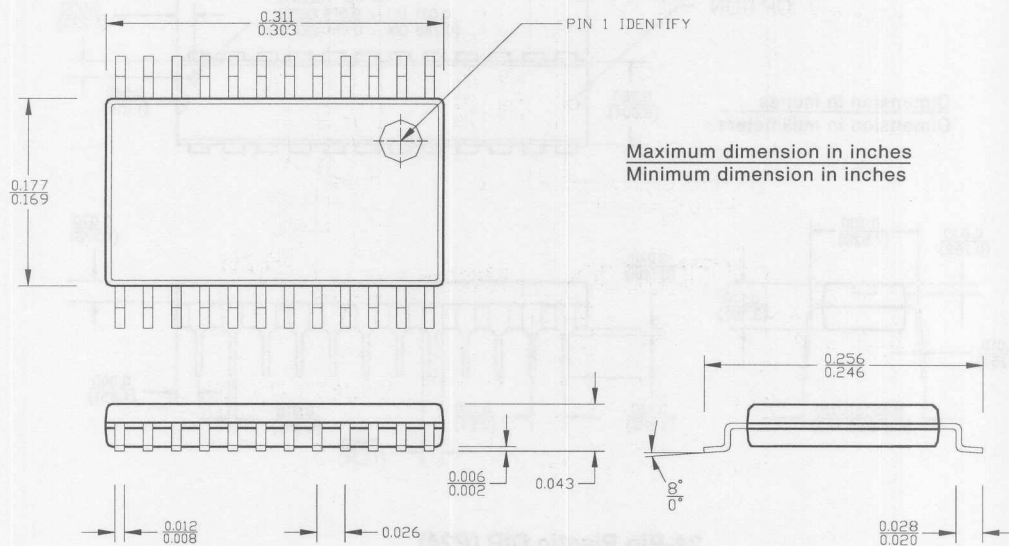
20-Pin TSSOP (T20)



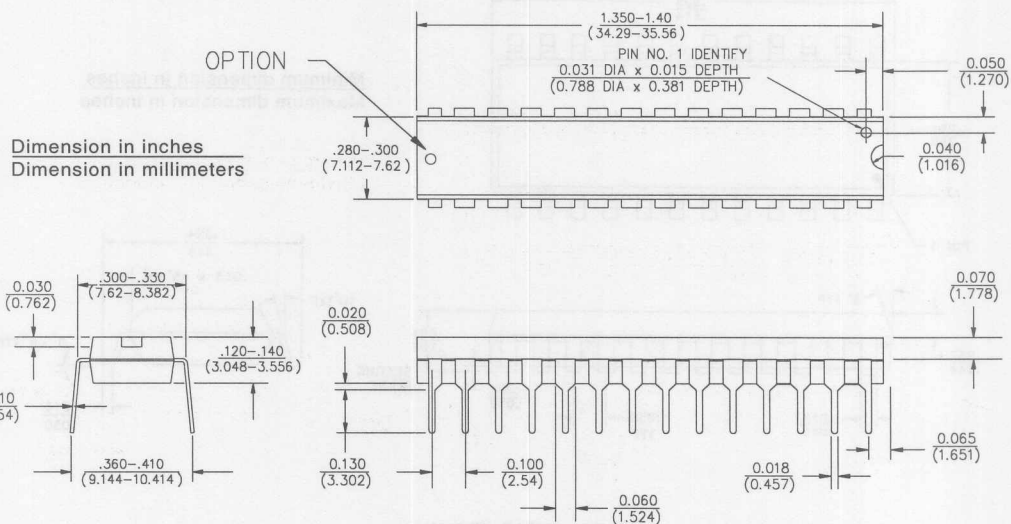
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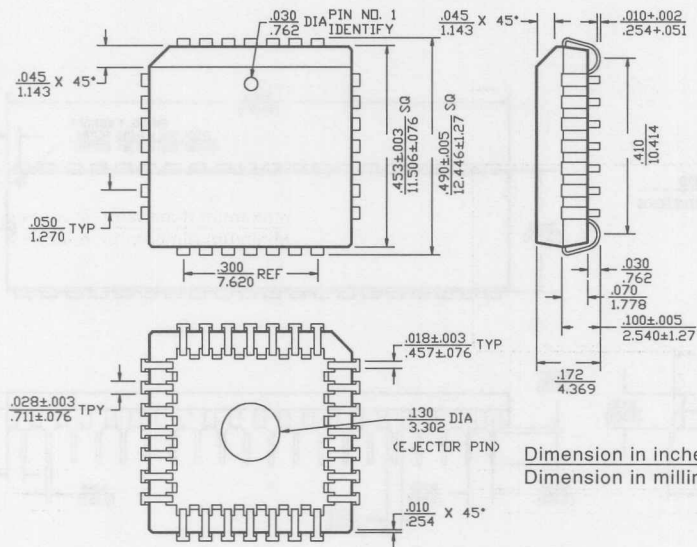
24-Pin SOIC (S24)



24-Pin TSSOP (T24)

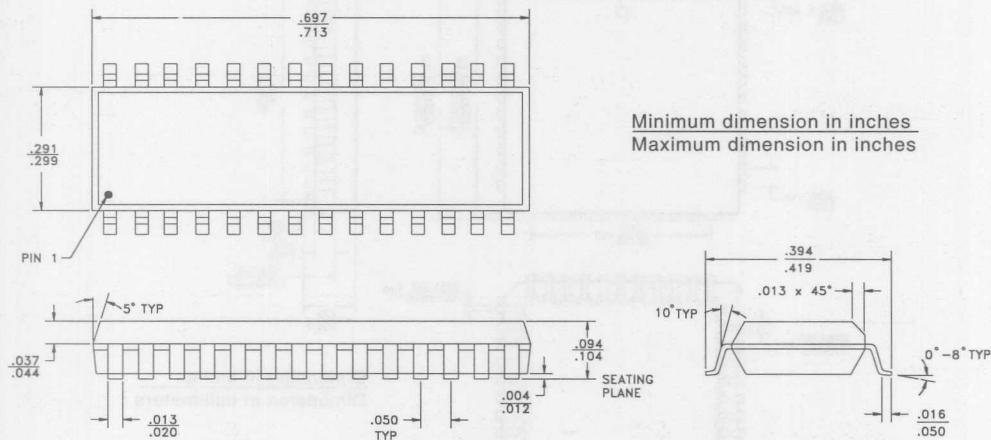


28-Pin Plastic Dip (P28)



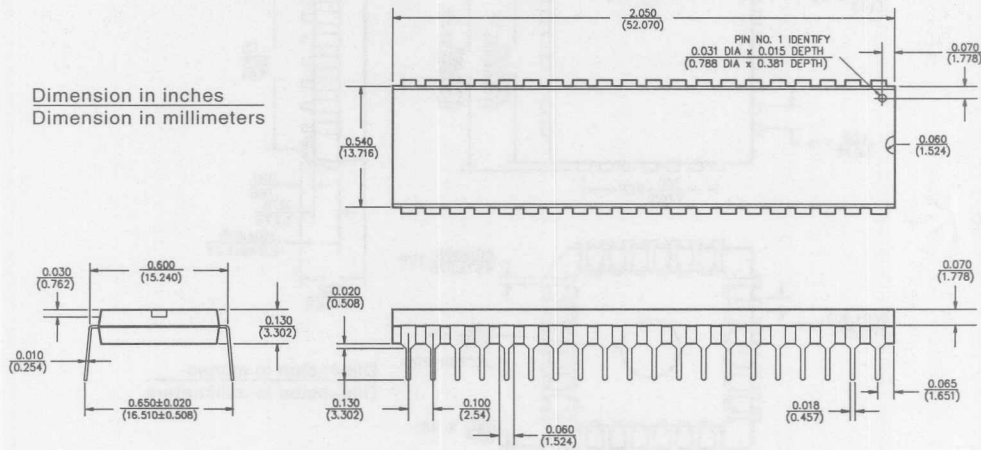
Dimension in inches
Dimension in millimeters

28-Pin PLCC (J28)

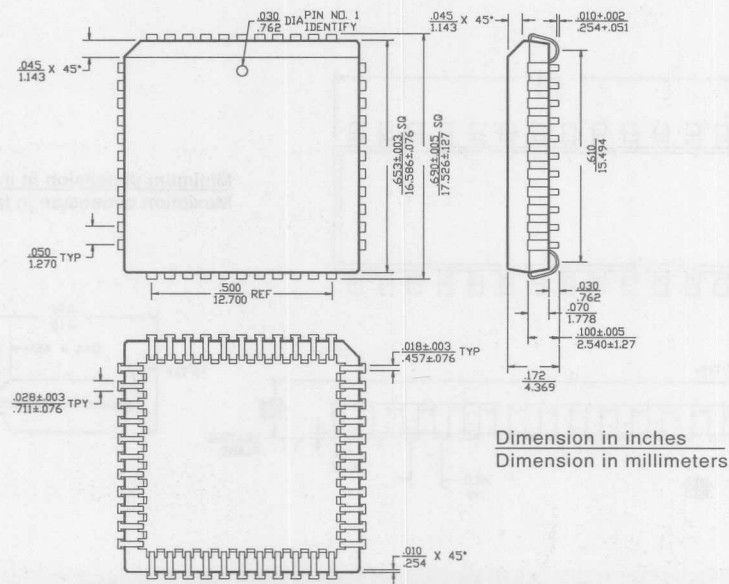


Minimum dimension in inches
Maximum dimension in inches

28-Pin SOIC (S28)



40-Pin Plastic DIP (T40)



Dimension in inches
Dimension in millimeters

44-Pin PLCC (J44)

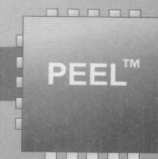


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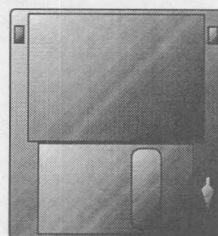


For PEEL Arrays
and Devices

1995 / 1996



*ICT's PLACE Development Software
is available free to qualified PLD users!*



*For more information contact your local ICT
representative as listed in Section A*

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Introduction to PLACE

Introduction to PLACE

- 1.1 PLACE Advanced Development Environment
- 1.2 PLACE Introduction
- 1.3 PEEL Device and PEEL API Support
- 1.4 Converting PEEL File to PLACE File
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Introduction to PLACE

8.0 Introduction to PLACETM

8.1 PLACE Advanced Development Software

Welcome to the PLACE Advanced Development Software from ICT, Inc. PLACE (PEEL Logic Architectural Compiler and Editor) is an enhanced development package that offers complete support for ICT's family of PEEL (Programmable Electrically Erasable Logic) Arrays and Devices.

The PLACE Advanced Development Software is free to qualified PLD users. To obtain a copy of PLACE please contact your local ICT representative (see Section A).

PLACE Features

Architectural Editor

PLACE incorporates an innovative architectural editor which graphically illustrates and controls the architectures, logic equations, state-diagram and truth-table entries, hence making the overall design easy to understand while allowing for optimum utilization.

Logic Compiler

The PLACE compiler performs logic transformation, allowing equations to be specified in a variety of formats. The compiler also features five levels of user-selectable logic reduction (including "auto-demorganization") making it possible to fit more logic into every design.

Logic Simulator

PLACE provides a multi-level logic simulator that lets the external and internal signals be fully simulated, analyzed and edited via a graphically illustrated waveform display.

Documentation

PLACE designs can be documented through batch printing of the logic design description, architecture and waveform displays.

Programmer Interface

Programming is supported by a direct interface to the ICT PEEL Development System programmers: PDS-1, PDS-2 and PDS-3, and by other popular programmers via the serial communication port or by automatically executing the third-party programming software from within PLACE.

8.2 PLACE Introduction

The PLACE Software portion of this description is organized in six sections. Before trying to design with the PLACE software, make sure you read through the three sections: "Introduction", "Installation" and "Getting Started". By doing so you will save yourself time.

After you have completed installing the PLACE software and have become familiar with the basic operations, you can refer to the "Operation Reference Guide" and "PLACE Design Language Reference Guide" section as you implement your first design. Documentation describing several application examples is provided in Chapter 13. These examples are also included on diskette and will automatically be loaded during installation.

While using this manual and the software you may need to reference the product specifications in the data book.



The software operations and features described in this manual are referenced to PLACE Version 2.71. For additional information on new features and manual corrections, please refer to the README.DOC file on the PLACE disk.

8.3 PEEL Device and PEEL Array support

The devices supported in the PLACE software include:

PEEL Arrays

PA7024

PA7128

PA7140

PEEL Devices

PEEL18CV8

PEEL20CG10A

PEEL22CV10A+

PEEL22CV8

PEEL22CV10A

PEEL22CV10AZ+

Additional devices will be supported in future software versions.

8.4 Converting APEEL File ".APL" to PLACE File ".PSF"

ICT has discontinued further development of its original PEEL software named APEEL. All products are now supported by PLACE. If you still use APEEL for development your designs can be converted to the PLACE design language format by using the APL2PSF (APL2PSF.EXE) utility. This allows the PLACE enhanced features available for the PEEL Arrays to be used to implement designs for the lower density PEEL devices.

The format for the APL2PSF utility is:

APL2PSF *filename*

The extension of the *filename* defaults to ".APL" if not specified.

8.5 JEDEC File Translation

The JEDEC-file translation utility of the PLACE Software translates JEDEC files created for programming other PLDs (PALs, GALs, EPLDs etc.) to JEDEC files used for programming PEEL Devices. (There is also a "smart translator" available on a separate disk which adds the capability to translate JEDEC files for other PLDs to JEDEC files for pin-compatible PEEL Arrays. See the data sheet in this data book and the "read me" file on the smart translator disk for more information.)

The translated JEDEC file will program a PEEL Device to be a pin-for-pin replacement for the original PLD. The utility translates JEDEC files that have been written on a disk. If a disk file is not available, the pattern may be read from a master device with ICT's PEEL Development System or a third-party programmer. When a third-party programmer is used, the software will allow the file to be up-loaded through a serial port and written to a file.

The translated PEEL JEDEC file is given the name of the original file with the ".JED" extension modified to ".JEX". The ".JEX" file can then be used to program your PEEL devices. The translator can be accessed directly from DOS or through the PLACE Utilities menu.

Using the JEDEC File Translator from DOS

The PEEL device translator program is contained in a file called PEELXLT.EXE on the program diskette. When using PEELXLT.EXE, you must specify a PLD source file name, a source PLD type, and a target PEEL device type. Type: "PEELXLT <source_filename> <source_PLD> <target_PEEL_device>". An example is given below:

```
PEELXLT B:\R8CNTR 16R8 18CV8
```

In the above example, the JEDEC file "R8CNTR.JED" (which is included on the disk as an example) is translated from a PAL16R8 to a PEEL18CV8 device. The translation process creates the PEEL device JEDEC file "R8CNTR.JEX". You need not specify the extension for the PLD source file name because it is assumed to have a ".JED" extension. Do not specify device family (e.g. PAL, PEEL, etc...) or manufacturer (e.g. AMD, Lattice, etc.) for source PLD and target PEEL device number.

Using the JEDEC File Translator from the PLACE Utilities Menu

After PLACE has been fully installed, the translator can be accessed from the "Translator" selection in the PLACE Utilities menu. Accessing the translator from PLACE, a sequence of menus are provided to aid in the translation process. From the first file menu, select Read/Translate and the file to be translated, then follow the menu-driven commands. Note that the translator is not mouse-driven, all commands must be selected from the keyboard.

These devices can be translated to the PEEL18CV8

PAL16L8	PAL16R8	PAL16R6	PAL16R4
PAL16P8	PAL16RP8	PAL16RP6	PAL16RP4
PAL10L8	PAL12L6	PAL14L4	PAL16L2
PAL10H8	PAL12H6	PAL14H4	PAL16H2
PAL16H8	PAL16LD8	PAL16HD8	PAL18P8
PAL18V8	GAL16V8	EP310	EP320
5C031	5C032	EP330	PAL18U8
PALCE16V8	85C220		

These devices can be translated to the PEEL22CV8

PAL20L8	PAL20R8	PAL20R6	PAL20R4
85C224	GAL20V8	PALCE20V8	

These devices can be translated to the PEEL20CG10A, PEEL22CV10A/A+

PAL20L8	PAL20R8	PAL20R6	PAL20R4
PAL20L10	PAL20L2	PAL18L4	PAL16L6
PAL14L8	PAL12L10	PAL22V10	PAL20G10
PAL20AP10	PAL20RP8	PAL20RP6	PAL20RP4
PAL20ARP4	PAL20ARP6	PAL20ARP8	PAL20ARP10
GAL20V8	PALCE20V8	GAL22V10	

These devices can be translated to the PA7024*

EP610	EP600	85C060	ATV750
-------	-------	--------	--------

This device can be translated to the PA7128*

PALCE26V12

These devices can be translated to the PA7140*

EP910	EP900	85C090
-------	-------	--------

* Requires Smart Translator from ICT Inc.

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- 9.3 Initializing the PLACE Software using "INIT" 9-4

PLACE Installation

9

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PLACE Installation

1. Select the location for the PLACE unit.
2. Read the installation instructions.
3. Mount the PLACE unit to the wall.

PLACE Installation

9.0 PLACE Installation

9.1 System Requirements

- ☐ IBM PC, XT, AT, 386, 486 or compatible
- ☐ Minimum 560K RAM memory for all designs
- ☐ EGA, VGA, SVGA or Hercules Graphics
- ☐ A hard disk with at least 4.0 MB free space
- ☐ Logitech or Microsoft mouse with driver
- ☐ DOS version 3.0 or greater
- ☐ (Optional) Expanded Memory with LIM specification version 3.2 or higher
- ☐ If using PDS-2 or PDS-3 programmer, one communication port (serial port)

9.2 Hard Disk Installation Procedure

- ☐ Turn the computer on.
- ☐ Boot-up DOS 3.0 or higher.
- ☐ Install your mouse driver, otherwise PLACE will not boot-up.
- ☐ Insert the PLACE disk into drive A. Do not write-protect this disk.
- ☐ At the A> prompt, type "INSTALL" followed by the [ENTER] key. Note: you can abort installation at any time by pressing Ctrl-Break.
- ☐ Type in your company name, address, date, and your name.
- ☐ Select your options. Enter the directory you want PLACE to be installed to. Default drive and directory is C:\ICTPLACE.
- ☐ Once installation is completed, type "INIT" to initialize the PLACE software. For subsequent use of the PLACE software, type "PLACE" followed by the [ENTER] key.
- ☐ (Optional) If you wish to run PLACE from any directory, you can do this by adding the following to your AUTOEXEC.BAT file. Assuming "C:\ICTPLACE" is the installed directory, you would add "C:\ICTPLACE" to your DOS path and insert "SET ICTPLACE=C:\ICTPLACE".
- ☐ ICT recommends that MS DOS 5.0 (or greater) users move TSR programs (e.g. PC pop-up calculator program) to high memory, so that the computer has enough conventional (low) memory to run the PLACE software. An example for loading TSR programs into high memory is:

LOADHIGH(LH) PC-CALC.EXE (to load PC-CALC.EXE into upper memory).

DOS will not tell you if the procedure is successful or not. If the procedure was not successful the program will occupy conventional memory. To check if the program was loaded into high memory enter the command MEM /C and note the program's location.

9.3 Initializing and Re-Initializing PLACE using "INIT"

After PLACE installation, the PLACE software can be initialized by typing "INIT" followed by the [ENTER] key in the PLACE directory. The initialization procedure erases the "PLACE.SAV" file which stores the set-up configurations of the PLACE software. Once this file is erased, the PLACE software (i.e., by typing "PLACE" followed by the [ENTER] key) sets all of the configuration variables during boot-up except for the color, graphic adapter (VGA only) and mouse type variables, to the default conditions.



You can re-initialize PLACE any time you run into problems with the software, or if you want to change the set-up configuration variables.

Mouse Type Option

The PLACE software allows multiple mouse cursor types to be displayed depending on the mode selected (e.g. Edit Eqn, Edit Arch, Label, etc.) in the Design module. For instance, a left-pointing arrow (" \leftarrow ") mouse cursor indicates the current mode is the "Edit Eqn" mode. Figure 9-1 illustrates the different mouse cursor types found in the Design operation. In addition, each of the PLACE operations has its own unique mouse cursor.

Programmer Type Option

The Place Software allows initialization of PDS series programmers (PDS-1, PDS-2, PDS-3).



Standard (Default) cursor used for most functions or modes.



Design Command Modes such as Label, Copy, Swap, Erase, Allocate and LCC Re-Assign modes.



Edit Equation mode.



This cursor indicates that the PLACE software is set to a "pause" condition, usually for reading error messages. Press any key or mouse button to continue.

Figure 9-1. Multiple Mouse Cursor Types



If you are experiencing mouse problems with the multiple cursor mode, ICT recommends selecting the single cursor type during the initialization procedure.

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Getting Started with PLACE

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Getting Started with PLACE

- 10-1. Installing PLACE software
- 10-2. Using the PLACE software
- 10-3. Loading PLACE
- 10-4. A Quick Tour through the PLACE software
- 10-5. The PLACE Design Process

Getting Started with PLACE

10.0 Getting Started with PLACE

10.1 Entering the PLACE software

Once PLACE is properly installed (i.e., PLACE was initialized by using "INIT"), it can be entered by typing "PLACE" while in the ICTPLACE directory. Pressing the ENTER key twice after typing "PLACE" will bypass the welcome message. If you wish to enter PLACE from any directory, see section 9.2 or 9.3 on "Hard Disk Installation Procedure". Before using the PLACE software, please read through the following sections on "Using the Mouse" and "Getting HELP".

10.2 Using the Mouse

The PLACE software and manual will commonly refer to several mouse actions using the nomenclatures specified in Table 10-1.

Term	Mouse Action
Click	press/release the left button of mouse
Click-R	press/release the right button of mouse
Click-LH	press/hold the left button of the mouse while moving the mouse
Click-RH	press/hold the right button of the mouse while moving the mouse
Click-MH	press/hold the middle button of the mouse while moving the mouse (3-button mouse only)

Table 10-1. Nomenclatures for PLACE mouse actions



Note that the default mouse cursor is a North-West pointing Arrow. However, several cursor types (Figure 9-1) may appear depending on whether option #1 of the mouse cursor types was selected during the PLACE initialization procedure (Section 9.4), or on the type of mode or function that was selected in the PLACE software.

"Click" - press/release left button

"Click" is used in all operations and modes to make a selection. A selection can be made by moving the mouse cursor to the desired item, and press/release the left button of the mouse. In many cases the selected item will be highlighted. Items that can be selected include pop-down and pop-up menu windows, architectural elements in the design operation such as Logic

Control Cells (LCC), I/O Cells (IOC), Input Cells (INC), Global Cells (GBC), test vector waveforms (Simulate operation), etc.

"Click-R" press/release right button

"Click-R" in most cases is used to exit, complete or return from the current function being performed. **In the Design operation, Click-R is also used to toggle back and forth from the default "Edit Architecture" mode to the "Edit Equation" mode.**

"Click-LH" or press/hold the left button while moving the mouse

Click-LH is used in both the Design and Simulate operations. In the Design operation, it is used to scroll from one LCC/IOC to another in the LCC/IOC screen. In the Simulate operation, it is used for panning in the waveform screen as well as block selection for the copy, move, and delete functions in the "Edit" mode.

"Click-RH" and "Click-MH" or press/hold the right and middle button respectively while moving the mouse

For 3-button mouse systems, click-MH (click-RH for 2-button mouse) is used to display the menu options in the PLACE text editor utilized in the Design or Program operation. While holding the middle mouse button down (right button for 2-button mouse), move the mouse cursor and click at the menu option. Once the option is selected, the middle button can be released.

Mouse support in the PLACE Text Editor

The mouse is supported in the PLACE Text Editors which are used within the Design, Compile and Program operations. To initiate the mouse support, press the middle button (3-button mouse) or right button (2 button mouse) of the mouse but don't release the button. Move the mouse cursor to the top of the screen to select the functions. Table 10-2 lists the mouse actions in the text editor.

Mouse Action	Function
Click within the text area	Move the text cursor to the mouse cursor
Click at the top border area	Scroll 6 lines up
Click at the bottom border area	Scroll 6 lines down
Click at the first line of the text	Scroll 1 line up
Click at the last line of the text	Scroll 1 line down
Click-R (right button)	Exit editor (3-button)
	Access mouse menu (2-button)
Click-M (middle button)	Access mouse menu (3-button only)

Table 10-2. PLACE Text Editor Mouse Actions

Re-initializing the mouse in PLACE

In the event a mouse problem is encountered, press the [ESC] key as many times as needed to exit the current mode or function and return to the main screen of the operation (Design, Compile, Simulate, Document and Program). Then, press the [Alt]-M keys (simultaneously press the [Alternate] and character "M" keys) to re-initialize the mouse.

10.3 Getting HELP

The PLACE software incorporates an on-line HELP feature which provides information and procedures for most PLACE functions and modes. To get HELP information, just point the mouse to the menu function or mode and simultaneously press the [F1] key. Besides this on-line command HELP, a general HELP menu is provided in the Utilities pop-down menu.

10.4 A Guided Tour through the PLACE software

To quicken the learning process, this section discusses some basic procedures commonly used in the PLACE software. The device used in this guided tour is the PA7024. Some of the terms used in this section may only be applicable to the PA7024 device (or the PEEL Array family of devices). For instance, terms such as LCC (Logic Control Cell) and GBC (Global Cell) pertain only to devices in the PEEL Array family.



If you are a first-time PLACE user, ICT recommends that you run the PLACE software while reading this section. By actually performing the instructions (specified in *italics*), you will be able to get a more complete understanding of the features, modes or functions found in the PLACE software.

There are five main operations that can be performed with PLACE: Design, Compile, Simulate, Document and Program. When first entering PLACE, it will default to the Design Operation in the edit architecture mode ("Edit Arch"). The display will show the PA7024 PEEL Array pin block diagram (Figure 10-1).



Note that PLACE automatically loads the ANEW template file upon initial boot-up. In Figure 10-1, the PLACE software has loaded the ANEW file (ANEW7024.PSF) for the PA7024 device. There is an ANEW template file for each device supported by the PLACE software. For instance, the ANEW7140.PSF file is the template file for the PA7140 device. Each ANEW file contains the device's default cell configurations.

At the top of the screen, there are five pop-down menu options: File, Design, Operation, Utilities and Options (available only in the Design operation). *Move the mouse cursor to the "Operation" menu.* A pop-down window will appear showing the five main operations (Figure 10-2). Note the menu option titled "Design" to the left of the Operation menu. This menu is called

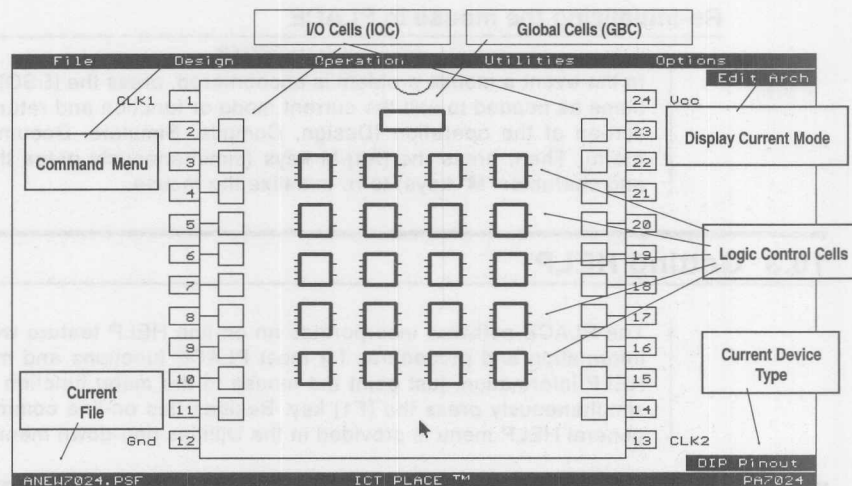


Figure 10-1. The PA7024 Pin Block Diagram screen in the Design Operation

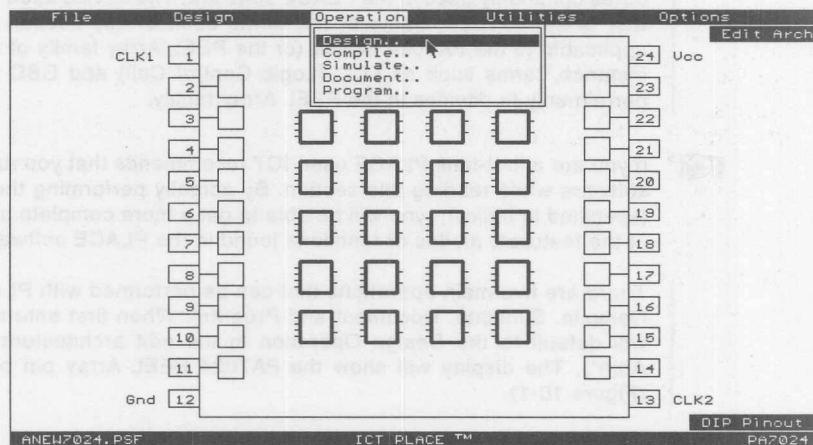


Figure 10-2. The Operations pop-down menu

the "command" menu. Each time a new operation is selected, this command menu will change to allow the selection of commands specific for that operation. The command menu is also used as an indicator for the current operation.

Move the mouse cursor to the "File" menu option and Click the "Read" command. A list of example PLACE Source Files (.PSF) will appear (Figure 10-3). The design examples provided with the PLACE software include:

- ☐ Multiple-Application Design Example (PA7024, DEMO1A.PSF)
- ☐ 8-Bit Counter with Hold, Reset and Preset (PA7024, COUNTER1.PSF)
- ☐ Bi-Directional I/O Port (PA7024, BI_PORT.PSF)
- ☐ Bus Programmable Clock Generator/Timer (PA7024, TIMER.PSF)
- ☐ Blackjack Machine Example (PA7024, JACK7024.PSF)
- ☐ Timer/Counter (PA7140, TC7140.PSF)
- ☐ 4-Bit State Machine with 8-bit Counter (PA7128, ST7128.PSF)
- ☐ Basic Gates (18CV8, V8GATES.PSF)
- ☐ Basic Registers and Latches (18CV8, V8REGS.PSF)
- ☐ Clock Divider and Address Decoder (18CV8, V8CLKADD.PSF)
- ☐ Bus Programmable 8-to-1 Multiplexer (18CV8, V8BUSMUX.PSF)
- ☐ 8-Bit Counter with Function Controls (18CV8, V8FCNTR.PSF)
- ☐ Change-of-state Input Port with Interrupt (18CV8, V8CPORT.PSF)
- ☐ Octal Synchronization Circuits (18CV8, V8SYNC.PSF)
- ☐ 8-Bit Up/Down Loadable Counter with Carry-out or Borrow-in (PEEL22CV10A, V10CNT8.PSF)
- ☐ 9-Bit Even/Odd Parity Generator/Checker (PEEL22CV10A, PARV10A.PSF)
- ☐ 8-Bit Change-of-State Input Port with Interrupt (PEEL22CV10A+, V10ZPORT.PSF)
- ☐ One-Hot State Machine (PEEL22CV10A+, ONE_HOT.PSF)



As shown in Figure 10-3, there are two methods of making a selection from the file menu window:

1. Click to highlight a file or directory, and then click at the [OK] selector.
2. "Double Click" at the file or directory. The first click highlights the selection, and the second click makes the selection.

Click the DEMO1A.PSF file. The PLACE Design operation will once again be displayed, but this time with the DEMO1A demonstration design file. For more detailed information on the demonstration example files refer to Chapter 13 of this manual.

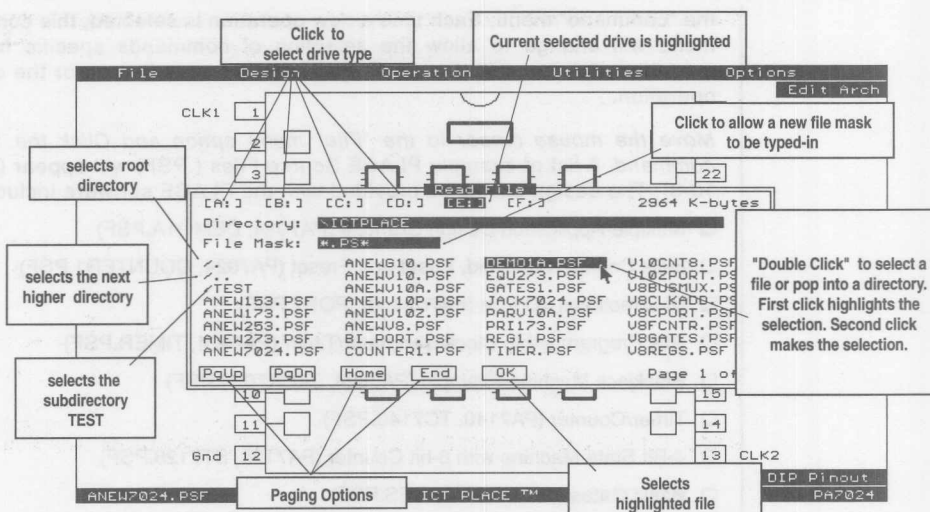


Figure 10-3. Reading a demonstration file from the File menu

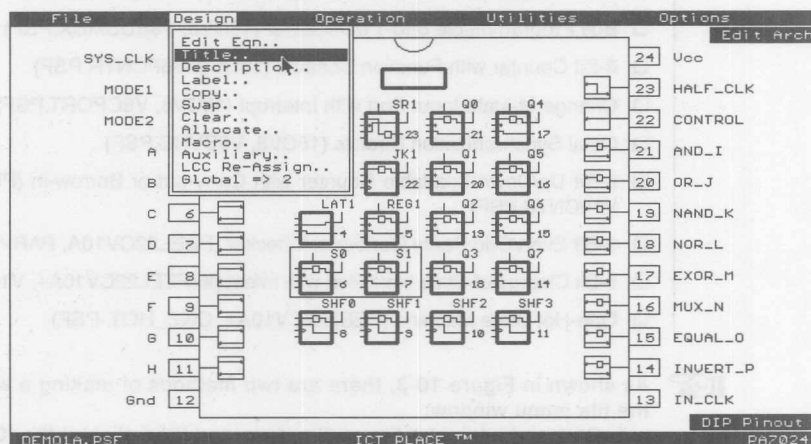


Figure 10-4. The "Design" command menu

Once the file is loaded, move the mouse to the "Design" menu option at the top of the screen (Figure 10-4). Click at the "Title" command. A window will appear on the screen displaying the title, designer and date of the design. The title of the design can now be entered by typing in the characters from the keyboard. Click or press the [Enter] key to move the cursor to the next Title field. Click-R or press the [Esc] key to exit this mode.

Move the mouse cursor back to the "Design" menu option and click the command listed as "Description". The screen will now display the description of the design (Figure 10-5). Move the mouse cursor into the displayed

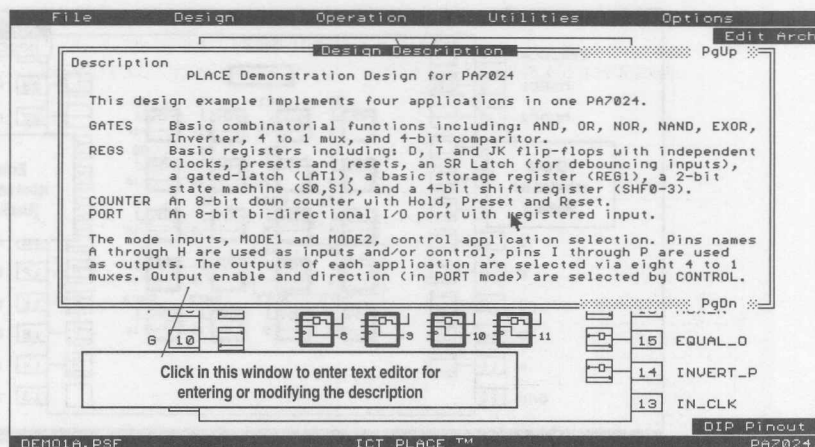


Figure 10-5. The "Description" window

window and click the mouse button. This procedure allows the design description to be entered or modified by having the PLACE software automatically open the text editor and highlight the text. *Press [Esc] to exit the text editor.*



With a 3-button mouse, click-R exits the text editor and returns to the previous screen. For the 2-button mouse system, click-RH (press and hold the mouse right button) to allow selection of the text editor menu at the top of the screen. Then while the right button is still held down, click at the "ESC" menu option to exit the editor. Please refer to Section 11-14 on "Text Editor Commands" for more information.

From the pin block diagram screen move the mouse cursor to the "Design" menu option and click the "Label" command. Notice that the mouse cursor changes from a North-West pointing Arrow to a Hand cursor (the Hand cursor is available only if option #1 of the mouse cursor type was selected during the PLACE initialization procedure). *Now move the cursor to one of the Logic Control Cells (LCCs), Input/Output Cells (IOCs), or Input Cells (INCs - PA7140 only) and click the mouse button.* A window will appear displaying the current label (or name). Figure 10-6 shows that I/O cell #2 was selected in the Label mode. To change the label use the [Back Space] key and type in the new label followed by the [Enter] key. The Label command is used to define all IOCs, INCs and LCCs that are used in a design.



The architecture of the LCCs, IOCs or INCs can be configured prior to labeling. However, labels must be specified before the equations, state-diagrams or truth-tables can be entered. Please refer to Chapter 11 "Operation Reference Guide" for options on the "Label" command.

Click-R to exit the "Label" mode and return to the "Edit Arch" mode. Now, move the cursor to one of the LCCs. Note that both the LCC and its interconnected IOC will be highlighted. *Click the mouse to bring up the*

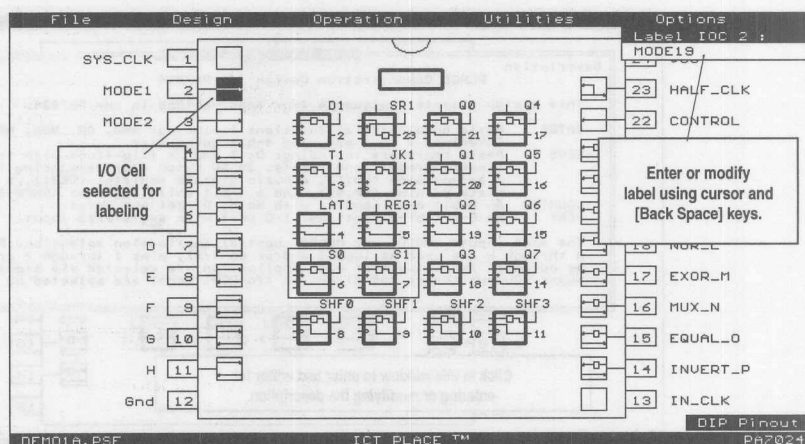


Figure 10-6. The "Label" command for Pin, INC, IOC and LCC

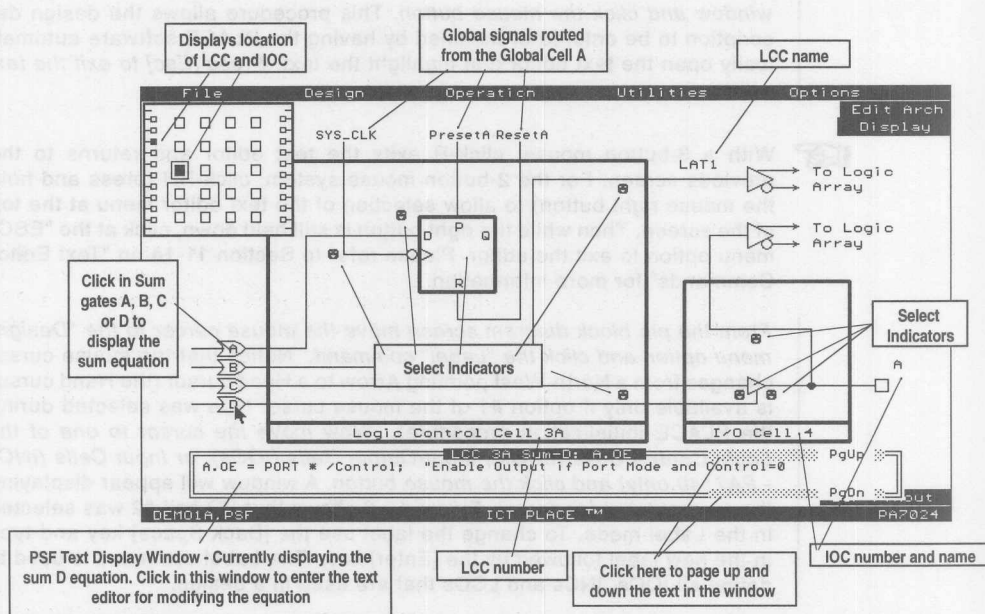


Figure 10-7. Configuring the LCC and IOC Architecture

associated "LCC and IOC Screen". This screen displays a close-up view of the selected LCC and its associated IOC configuration.

Select the configuration of the cells by clicking at any of the "select indicators" (Figure 10-7). With the PA7024 device, over 4000 configurations can

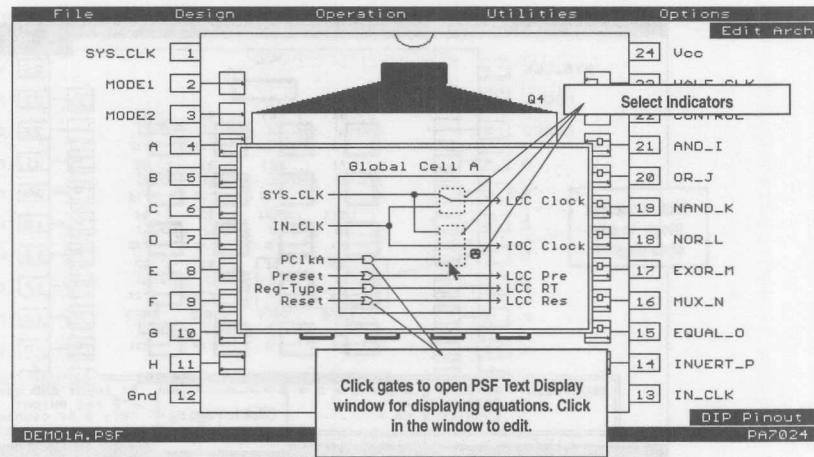


Figure 10-8. Configuring the Global Cell A (GBC) Architecture

be selected by clicking at each of the select indicators. Any time the mouse cursor is moved away from a select indicator, the pop-up window is cleared. *Click-LH (press/hold left mouse button) and move the cursor left and right or up and down.* This allows panning from one cell to another without returning to the pin block screen. Notice that the miniature pin block diagram in the upper left corner displays the current LCC/IOC location.

Move the cursor into the "D" OR or Sum-D gate (shown in Figure 10-7) and click the mouse button. A window displaying the equation for the selected OR gate will be opened. This window will be referred to as PSF Text Display Window. The size of the window can be increased or decreased by pressing the [Up] or [Down] cursor key, and followed by the [Enter] key (refer to Chapter 11 "Operation Reference Guide" for more information on the PSF Text Display window). *Click-R to close the display window. To return to the pin block diagram screen, click-R once again or press the [Esc] key.*

The Global Cell (GBC) configuration can be selected by the same process, i.e. by clicking the select indicators in the cell (Figure 10-8).



There are multiple global cells in all PEEL Arrays. For instance, the PA7024 device has two global cells which are called Global Cell A and B. The default condition for the PA7024 (and all PEEL Arrays) is the one global cell mode. The two global cell mode can be selected by clicking at the "Global = 2" command found in the "Design" menu window. With two global cells, Global Cells A and B control global signals for all LCCs connected to the IOCs located on the left (pins 2 to 11) and right side (pins 14 to 23) of the pin block diagram respectively. Please refer to the PEEL Array data sheet for more information on the global cells.

In the pin block screen, move the mouse cursor to the "Design" Command pop-down menu again. Click the command listed as "Edit Eqn" for edit equation. Notice that the mouse cursor has changed to a "<-" (arrow) which is the Edit Equation cursor. Move the cursor to one of the four inputs of any

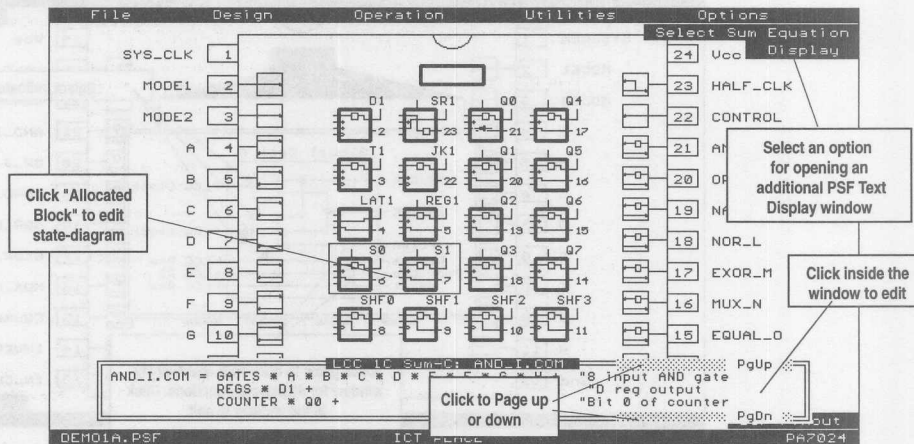


Figure 10-9. Selecting equations from the block diagram screen

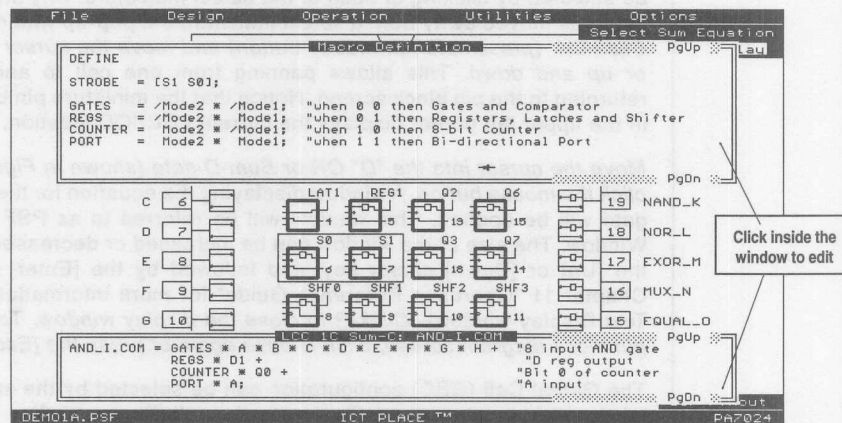


Figure 10-10. Selecting equations from the block diagram screen

LCC and the input will be highlighted. Click to select the input equation. In Figure 10-9, the PSF Text Display window displaying the sum-C equation was selected from the third input of the LCC "QO".

Move the mouse cursor to the "Display" option located in the upper right corner of the screen and click the mouse button. This opens a window listing the options for opening an additional PSF Text Display window. Move the cursor to highlight the "Macro Definition" option and click the mouse button. The PSF Text Display window showing the macro definitions specified in the design will appear (Figure 10-10).

Move the cursor to the inside of the PSF Text Display window and click the mouse button. This enters the text editor which is used for editing boolean


```

Press and hold middle button for mouse support
48 25
REG1.AP = Regs * D; "D Register, B=synchronous Preset
B.COM = OR J; "B output if in port mode (see output enable)
B.OE = PORT * /Control; "Enable Output if Port Mode and Control=0
Q0.T = 0; "Unused here, used for State-machine design STROBE
Q0.AP = 0; "Unused here, used for State-machine design STROBE
C.COM = NAND K; "C output if in port mode (see output enable)
C.OE = PORT * /Control; "Enable Output if Port Mode and Control=0
S1.T = 0; "Unused here, used for State-machine design STROBE
S1.AP = 0; "Unused here, used for State-machine design STROBE
D.COM = NOR L; "D output if in port mode (see output enable)
D.OE = PORT * /Control; "Enable Output if Port Mode and Control=0
SHF0.D = Regs * C; "Shift Register Bit 0
E.COM = EXOR M; "E output if in port mode (see output enable)
E.OE = PORT * /Control; "Enable Output if Port Mode and Control=0
SHF1.D = Regs * SHF0; "Shift Register Bit 1:
F.COM = MUX N; "F output if in port mode (see output enable)
F.OE = PORT * /Control; "Enable Output if Port Mode and Control=0
SHF2.D = Regs * SHF1; "Shift Register Bit 2:
G.COM = EQUAL O; "G output if in port mode (see output enable)
G.OE = PORT * /Control; "Enable Output if Port Mode and Control=0
SHF3.D = Regs * SHF2; "Shift Register Bit 3:
H.COM = INVERT P; "H output if in port mode (see output enable)
H.OE = PORT * /Control; "Enable Output if Port Mode and Control=0
Q0.T = COUNTER * "Bit 0 of Counter, B = HOLD
Q0.AP = COUNTER * A; "Input A presets Counter
AND1.COM = GATES * A + B * C + D * E * F * G * H + "8 input AND gate
AND1.OE = REGS * D1 + "D reg output
COUNTER.A = Q0 + "Bit 0 of counter
AND1.OE = Control; "Control is used to enable outputs I-P
Q1.T = COUNTER * "Bit 1 of Counter, B = HOLD
IB = !Q0;
F2=Save Esc.Click-R=Exit F1=Help Block: F7=Begin F8=End F9=Copy

```

Figure 10-11. Inside the PLACE text editor

equations, state diagram and truth table syntax. The selected equation will be highlighted (Figure 10-11). Note that equations can also be selected for the LCC/IOC screen by moving the cursor to the one of the four "Sum" inputs and clicking the mouse button (Figure 10-7). Equations for the Global Cell can also be selected this way (Figure 10-8). Once inside the editor, most of the standard Wordstar™ commands can be used. *Click-R* or press the [Esc] key to return to the pin block diagram screen again.

After returning from the text editor, the "Edit Eqn" mode is still selected (indicated by the "<" mouse cursor). *Click-R* and the cursor will change back to the default "Edit Architecture" cursor. *Click-R* will toggle back and forth between Edit Equation and Edit Architecture for quick access to both modes.

If you have followed the instructions up to this point you have now familiarized yourself with the basic functions of the Design operation in the PLACE software. Now, move the cursor to the "File" menu option and click the "SaveAs" command. The file window will appear (Figure 10-12). Move the cursor to the box named "NEW" and click the mouse button. Type in the name "TEMP" or any other new name to save your modified file. If the file extension is omitted, then it will be defaulted to ".PSF".

Once your Design file is saved, select the File pop-down window again and read in the "GATES1.PSF" design example. Move the mouse cursor to the Operations pop-down window and try selecting the other operations starting with Compile, Simulate, Document, Program and back to Design. The screens should look as displayed in Figures 10-13 through 10-16. For more information on the commands and functions for the five main operations, please refer to the "Operation Reference Guide" in Chapter 11.

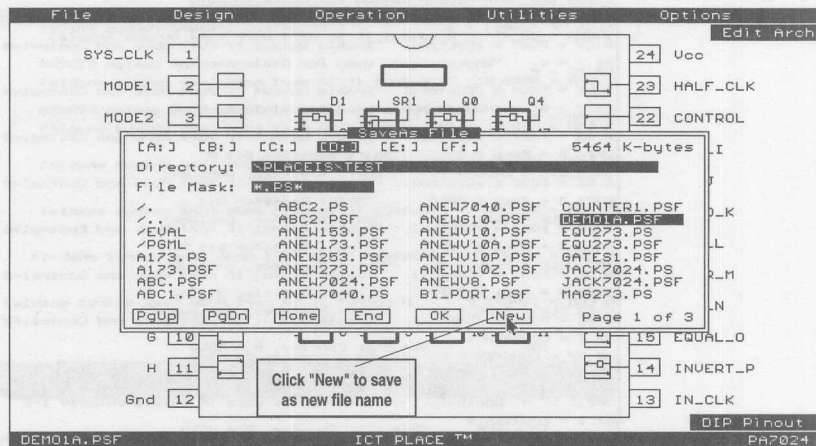


Figure 10-12. Using "SaveAs" to save a new PLACE source file

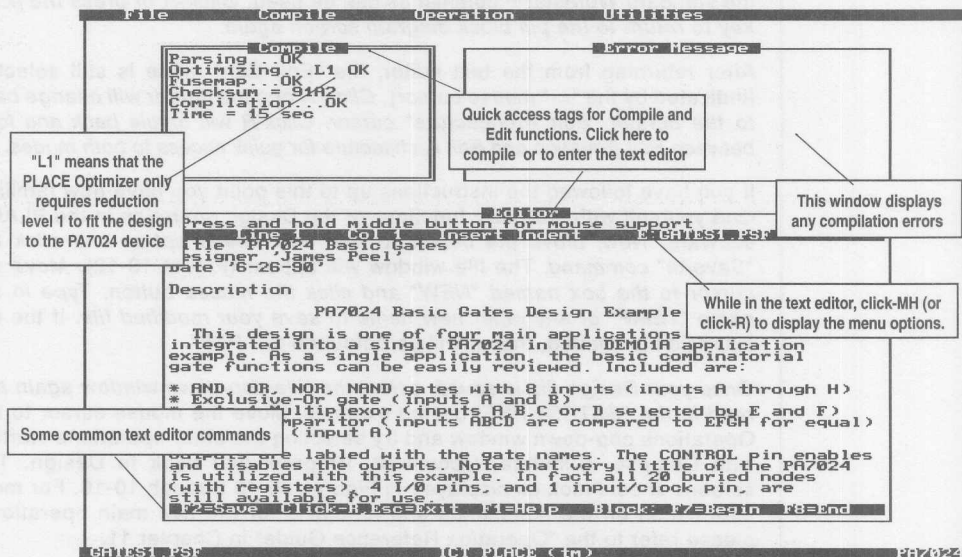


Figure 10-13. The Compile Operation Screen (Standard version only)

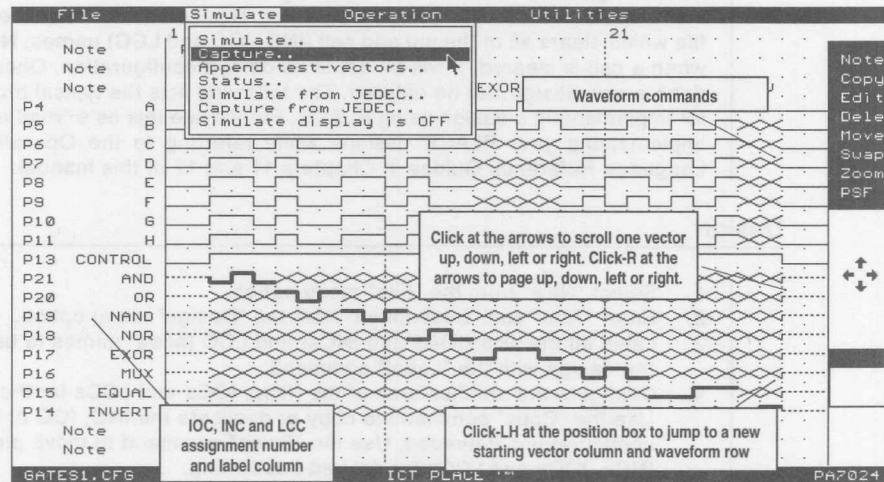


Figure 10-14. The Simulate Operation Main Screen

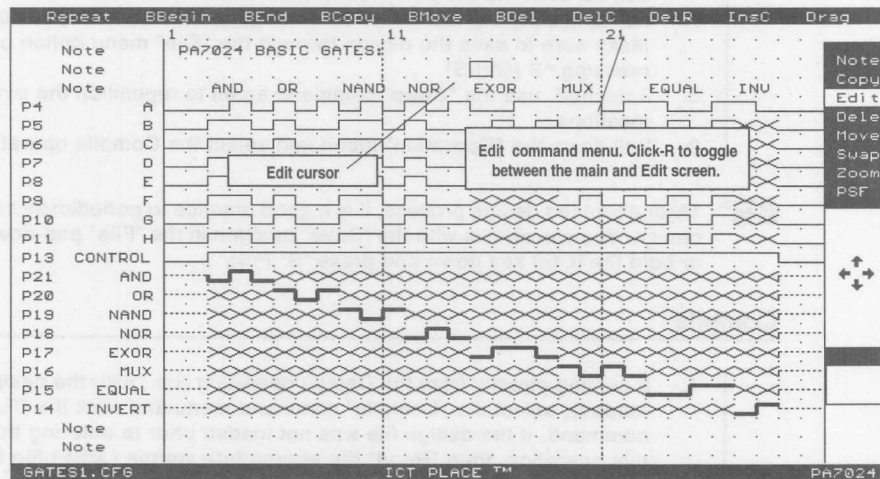


Figure 10-15. The Simulate Operation "Edit" Screen

10.5 The PLACE Design Process

New designs can be started by selecting the "New" command in the "File" menu option while in the Design Operation. This command loads the ANEW file which clears all of the pin and cell (INC, IOC and LCC) names. Note that when a cell is cleared, it will be set to its default configuration. Once this is done a new design can be entered. The following lists the typical procedure for implementing a design using PLACE. Please use this as a "road map" for implementing your PLACE designs while referring to the Operation and Language Reference Guides in Chapters 11 and 12 of this manual.

Design

1. Select "New" from the "File" menu option.
2. Enter "Title" and "Description" from the "Design" menu option.
3. Label all the pins (IOCs and INCs) and LCC (node) names to be used in the design with the "Label" command.
4. Configure the architectures of the INCs, IOCs and LCCs for the design. Use the "Copy" command to copy or duplicate the INC, IOC or LCC configurations if needed. Use the "Swap" command to move pins, INCs, IOCs and LCCs for desired positioning.
5. For state-diagrams and truth-tables, use the "Allocate" command to allocate the labeled IOCs and/or LCCs for the state machine and truth-table designs.
6. For boolean equation design entry, select the Edit Equation ("Edit Eqn") mode and enter the equations for each LCC input. The equation entry can be done via the pin block or LCC and IOC screen.
7. Edit or modify the architectures and equations until ready to compile. Make sure to save the design through the "File" menu option or by pressing ^S (Ctrl-S).
8. If desired, use the "Swap" command again to reposition the pin and cell locations.
9. Pull down the "Operation" menu and select the Compile operation.



Throughout the design process, it is a good practice to periodically save your design. You can do this with the "Save" function in the "File" pop-down menu or hold the [Ctrl] key down and press "S" (^S).

Compile

1. If coming directly from the Design operation (i.e., with the design file loaded), select the "Compile" command menu and click the "Run" command. If the design file was not loaded prior to entering the Compile operation, then "Read" the appropriate source (.PSF) file from the "File" menu window.
2. If a compile error occurs, the compiler will indicate the error with a message and locate the error in the displayed source file. You may analyze the error and correct it with-in the compile operation (by clicking the "Editor" title bar to enter the editor). You may also return to the

Design operation to correct the error. If the compilation is successful, proceed to the Simulate operation.

Simulate

1. Enter the input pin waveforms using the "Edit" command.
2. Enter expected output wavforms for test verification or use the "Capture" command in the "Simulate" menu window to automatically generate the output waveforms.
3. After simulation, click on the "Status" command to check if there are any simulation failures. Correct all simulation failures either by changing the vectors, or by returning to the Design operation and modifying the design.
4. Once properly simulated, append the vectors to the JEDEC file using the "Append test vectors" command from the "Simulate" menu window.
5. Save the ".CFG" simulation file using the "File" menu window. Like the design operation, periodically save your simulation (.CFG) files by pressing "AS". ICT recommends saving your first simulation vector file with the ".CFG" file extension. Any vector file can be saved with the extension ".CFx", where x is an alphanumeric character.

Document

1. In the Document operation, select the printer type and interface if you are running the PLACE Document operation for the first time.
2. Select the Batch or Single option.
3. Click in all the desired print options, such as pin block diagram, PLCC package pinout, cell architectures, simulated waveforms and design texts (such as equations, state-diagrams or truth-tables).
4. Once the options are selected, click the "Print" command to send the documents to the printer.
4. Save your selections onto your hard disk. The filename will consist of the root filename with the extension ".PRT".

Program

If using a PDS series programmer (PDS-1, PDS-2, PDS-3) refer to your PDS user's manual for the "program" operation. The "PC Com" (Serial Communication Port Window) Interface window is automatically displayed if the PDS Series Programmers are installed in your computer. The commands in the window allow the JEDEC file to be transmitted or received via the com port to or from a third-party programmer which has a serial communication file transfer utility.

Design operation is correct the error. If the compilation is successful, proceed to the Stimulate operation.

Stimulate

1. Enter the input pin waveforms using the "Edit" command.
2. Enter expected output waveforms for test verification or use the "Capture" command to the "Stimulate" command window to automatically generate the output waveforms.
3. After completion, click on the "Status" command to check if there are any simulation errors. Correct all simulation failures either by changing the vectors or by re-running the Design operation and modifying the design.
4. Once properly simulated, save the vectors to the JEDEC file using the "Export test vectors" command from the "Stimulate" menu window.
5. Save the "CFG" simulation file using the "File" menu window. Like the design operation, periodically save your simulation (CFG) files by pressing "F5". I/O recommendations specify that first simulation vector file save the "CFG" file extension. Any vector file can be saved with the extension "CFG", where x is an alphanumeric character.

Document

1. In the Document operation, select the printer type and interface if you are running the PLICE Document operation for the first time.
2. Select the Single or Single action.
3. Click in all the desired print options, such as pin block diagram, PLICE package diagram, pin connections, simulated waveforms and design tests (such as equations, state diagrams or truth-tables).
4. Once the options are selected, click the "Print" command to send the documents to the printer.
5. Save your selection onto your hard disk. The filename will consist of the root filename with the extension ".PRT".

Program

Using a PDS editor on computer (PDS-1, PDS-2, PDS-3) refer to your PDS user's manual for the "program" operation. The "PC Code" (Binary Command) (action Port Window) interface window is automatically displayed if the PDS Series Programmer is installed in your computer. The commands in the window are in the JEDEC file in its transmitted or received via the com port to or from a third party programmer which has a serial communication line transfer only.

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11.0 Operation Reference Guide

In this section, the features of the PLACE software are discussed in more detail. Sections 11.1 to 11.3 detail the features or functions that are similar in all PLACE operations. Features specific to each operation are discussed in the following sections.

11.1 File Menu

The "File" menu option shown in Figure 11-1 provides options for file maintenance, displaying system information and screen dumping to IBM/Epson printers (additional printers are supported in the Document operation). This file menu is similar in all operations (e.g., Design, Compile, Simulate, Document and Program operations) with the exception of the type of file (see Table 11-1 for PLACE file types) that is read or saved.

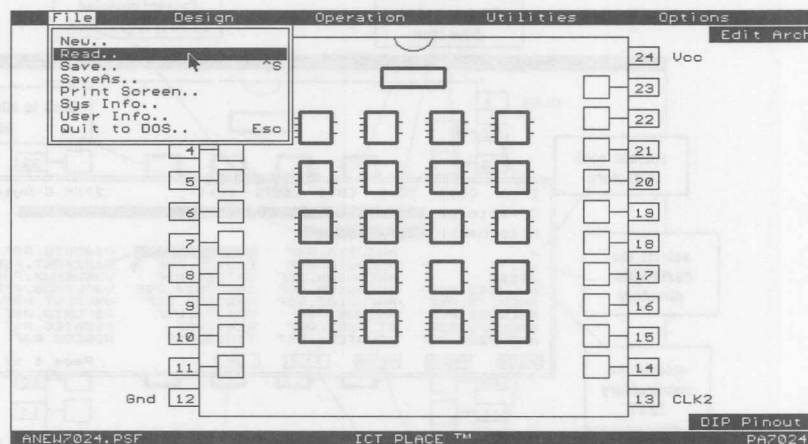


Figure 11-1. File Menu Option

- New** When in the Design operation, "New" clears the file in memory and allows device selection for starting a new design. It loads "ANEWxxxx.PSF" (xxxx = device number) as a template file. The PLACE software automatically prevents your edited ANEW file from overwriting the original file by prompting for a new file name during the "Save" command.
- Read** Allows a PSF source, simulation, documentation or JEDEC file to be loaded from the current directory in the current operation (e.g. loads PSF file in Design operation, CFG in Simulate operation, etc. - refer to Table 11-1). When

selected, the File selection window will appear (Figure 11-2):

- A file can be read by clicking the desired file name and clicking the [OK] selector. For quick selection, you can "double click", i.e., click twice on the same file name (first click highlights the file, and the second click selects the file).
- A new drive is selected by clicking the drive letter at the top of the directory window.
- A new directory is selected by clicking the directory name preceded by a "/", or clicking the "/" (next higher directory) or "/" (root directory). The selection action is similar to selecting a file, i.e., click the [OK] selector or "double click" the selection.
- A new file mask can be changed by clicking the file mask highlighted area and typing in the file mask. Use the [Backspace] key, cursor keys or the mouse to move the text cursor. Press the [Enter] key or click the mouse when completed. The default is "*.PS*". After the file is read, the name will appear in the lower left corner of the pin block screen.

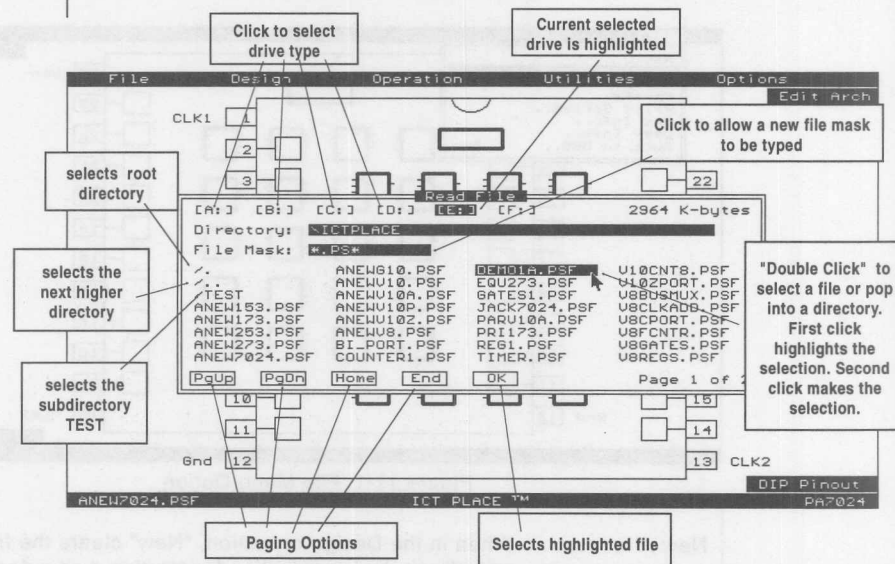


Figure 11-2. "Read" file selection screen

Save..... Saves the current file to disk. If the file is a new design (i.e. an ANEW file), then a new file name will be prompted for.

- SaveAs** Allows a new file to be saved to the current directory and disk. Click an existing file to over-write or click [New] selector to enter a new file name (the "SaveAs" file selection screen is similar to that of the "Read" screen in Figure 11-2 with the exception of the [New] function).
Note that in the Simulate operation if the root name of the CFG simulation file is not changed, then the file will still reference the same PSF design file. An example is shown below.
 DEMO1A.CFG saved as DEMO1A.CF1 - both files reference the DEMO1A.PSF design during simulation.
 DEMO1A.CFG saved as DEMO1B.CFG - these files reference DEMO1A.PSF and DEMO1B.PSF design respectively during simulation.
- Print Screen** Sends the current screen to the IBM or Epson graphic printer. For more printer support such as HP Laserjet and Postscript printers, please refer to the Document operation.
- Sys Info** Displays system information such as the file name, current directory, memory usage, etc.
- User Info** Displays information about the user, such as company name and address, user's name and date of installation.
- Quit to DOS** Quits the PLACE program and returns to DOS.

File Extension	Function
PSF	PLACE Source File (PSF) is the design source file used by the Design and Compile operations.
PS	Back-up file for the PSF design file.
MAP	Output file from the PLACE Compiler. This file provides detailed information on how the design equations are mapped into the JEDEC file. This information may be useful for design debugging.
RED	Output file from the PLACE Optimizer (prior to fuse mapping) in the Compile operation. This file contains the reduced or optimized equations in sum-of-products form. It maintains the PLACE design format so that it can be read into the Design operation for design verification and debug, or into the Document operation for documentation purposes. Note that the unused equations are omitted, so you will get "Equations not found" errors in the Design operation.
JED	Output JEDEC file from the PLACE Compiler used by the Simulate and Program operations.
JE	Back-up for the JED file.

Table 11-1. PLACE File Types

INT	Output file from the PLACE Compiler. This file contains the IOC and LCC interconnects which are used for the waveform display in the Simulate operation.
CFG	Primary vector source file for the Simulate operation. This file contains the data for vector simulation and waveform display. The PLACE Simulator simulates the vector in the CFG file with reference to the PSF design file with the same root file name. Hence, other file extensions may be used for the vector source file instead of CFG. However, we recommend using the CFG extension for your primary source file because all PLACE operations automatically reference the CFG file during the operation switching process.
CF(n)	(Recommended) Alternate vector source file for the Simulate operation. The character "n" can be any alphanumeric character except of course "G". This file extension method is used for the convenience of displaying all the vector files in the directory pop-up window, i.e., with the file mask *.CF*. Remember that the vector source files with the same root file name reference the same PSF design file. Example, the DEMO1A.CFG and DEMO1A.CF1 are vector files for the DEMO1A.PSF design file.
PRT	Input file for the Document operation. This file contains print selection tags for documenting the design.
PR	Back-up for the PRT file.
PN1	Default file extension for the output file from the PLACE Document operation (any file extension can be used with the exception of those that are specified in this table). The Document operation has a "Print to file" option which directs the screen capture data to this file. This file can then be sent to the printer using the DOS Copy command.

Table 11-1. PLACE File Types (Continued)

11.2 Operation Menu

When an operation is selected from the "Operation" menu (Figure 11-3), the PLACE software automatically loads the proper input file for the selected operation. For instance, the PSF file is loaded for the Design and Compile operations, the CFG file for the Simulate operation, the PRT file for the Document operation, and JED (JEDEC) file for the Program operation.

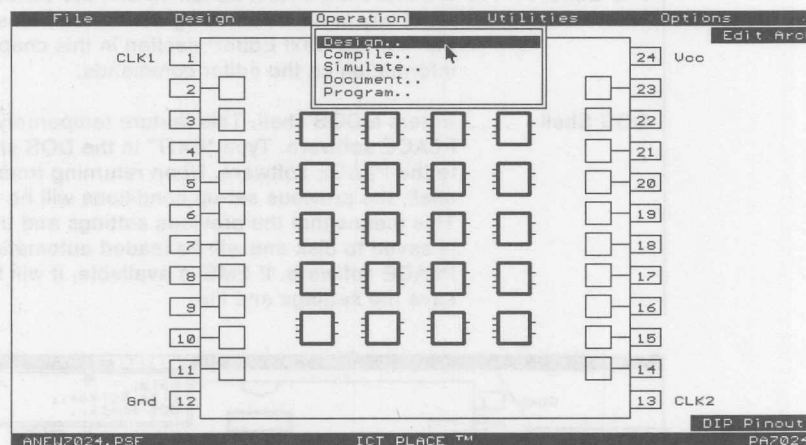


Figure 11-3. Operation Menu Option

- | | |
|----------------|--|
| Design..... | Selects the Design operation for creating a PSF design source file. The PSF file (if it exists) will automatically be loaded. |
| Compile..... | Selects the Compile operation for compiling the PSF design source file to create a JED (JEDEC) file for simulation and programming use. The PSF file (if it exists) will automatically be loaded upon entering the Compile operation. |
| Simulate | Selects the Simulate operation for creating a CFG vector source file which can be edited and simulated to the JED file. The CFG file (if it exists) will automatically be loaded. |
| Document | Selects the Document operation for documenting the design via printing the graphic screens and text files. If it exists, the PRT file will automatically be loaded. If the PRT file does not exist, then the print selection tags will be set to the default settings. |
| Program | Selects the Program operation for programming a PEEL Array or PEEL Device with the JED (JEDEC) file. The JED file (if it exists) will automatically be loaded. |

11.3 Utilities Menu

- Help** Provides general information on the Help instruction. For individual Help on each command, move the mouse to the command in the menu window and press the [F1] key. See Figure 11-4 for additional Help locations.
- File Editor** Enter the file or text editor. To exit the editor press the [Esc] key or click-R if using a 3-button mouse. Refer to the "PLACE Text Editor" section in this chapter for more information on the editor commands.
- DOS Shell** Enters a DOS shell. This feature temporarily exits the PLACE software. Type "EXIT" in the DOS shell to return to the PLACE software. Upon returning from the DOS shell, the previous set-up conditions will be restored. This means that the previous settings and the edited file is saved to disk and will be loaded automatically into the PLACE software. If EMS is available, it will be used to save the settings and file.

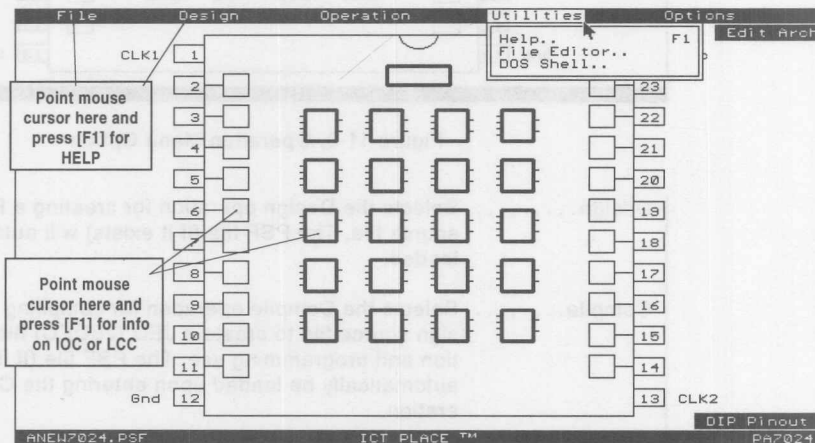


Figure 11-4. Utilities Menu Option

11.4 Design Operation - Design Menu

The "Design" menu contains commands used for implementing PEEL Array and PEEL Device designs. Note that some design commands, such as "LCC Re-assign" and "Global => 2" commands, are only applicable to PEEL Array designs. The two cursor types used by some of the commands in the "Design" menu are the "Left Arrow" and "Hand" cursors.

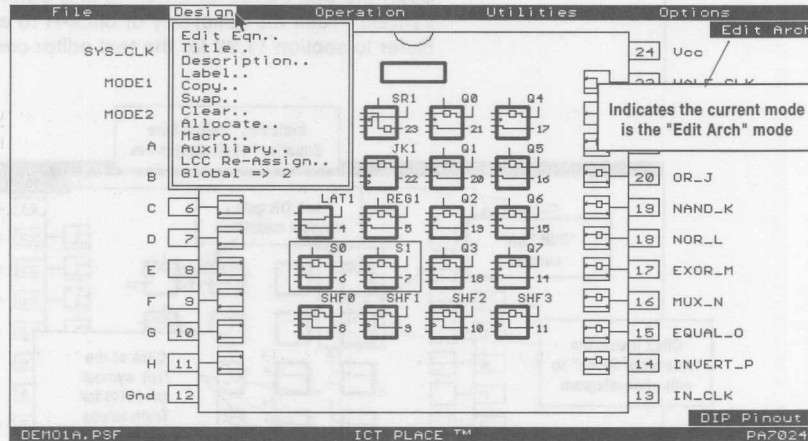


Figure 11-5. Design Menu Option



In the PLACE software, all commands that are not applicable to the selected device will be disabled.

Edit Eqn Selects Edit Equation mode (also selected by clicking-R in the Edit Architecture mode). This mode is identified by the left arrow mouse cursor (<-) if a 3-button mouse is used. In the "Edit Eqn" mode (also referred to as the "Select Sum Equation" mode), there are three ways of entering a logic description.

1. **Equation:** Move the cursor to highlight the OR (Sum) gate, and click to bring the sum equation out. Note that the equations for each cell are created by the label command. Hence, all cells must be labeled prior to selecting their OR gates.
2. **State diagram:** Move the cursor into the state diagram box without highlighting any of the OR gates in the LCC selected for the state diagram design. Then, click to open the window with the state diagram syntax. The requirement for designing with the state diagram syntax is that the cells (LCCs and IOCs) must be allocated using the "Allocate" command.

3. **Truth table:** Click at the T(n) labels located at the bottom of the LCC or IOC to open the window for displaying the truth table design syntax. Like the state diagram design, cells used in the truth table design must first be allocated.

After opening the window to display the design syntax (this window will be referred to as the **PSF Display window**), move the cursor into the window and click to open the text editor for entering and editing the design syntax. Press the [Esc] key or click-R to exit the editor. Refer to section 11.29 for the text editor commands.

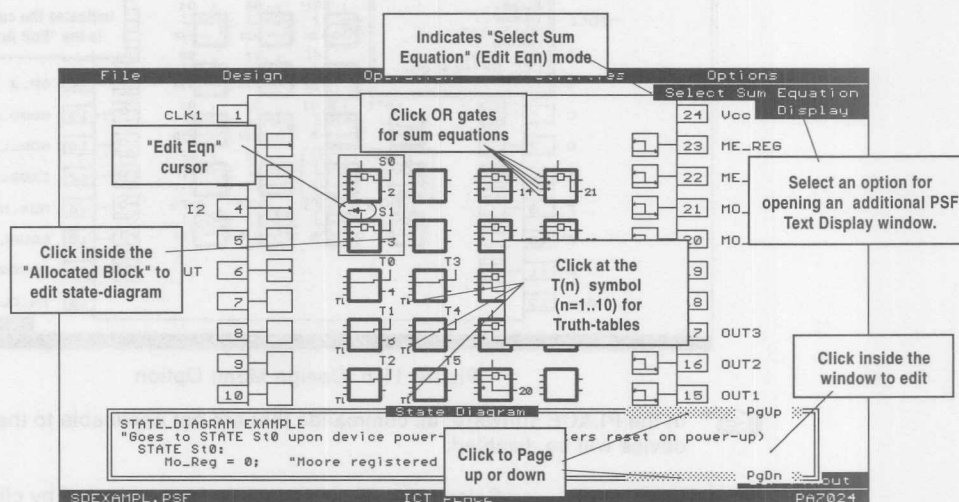


Figure 11-6. Edit Equation Mode

Title Allows a title, designer's name and date to be entered into the source file.

Description Opens a window to display the design description. The window size can be adjusted by pressing the Up or Down cursor keys followed by the ENTER key, or using the "Display" menu (see Section 11-6). Paging can be accomplished by clicking at the PgUp or PgDn markers, or using the PgUp or PgDn keys. To enter the PLACE text editor for editing, click inside the displayed window. There is no limitation in terms of the type of characters you can use for describing your design, just as long as your description is specified within the reserved words "DESCRIPTION" and "END_DESC". Note you can use the reserved word "DESCRIPTION" but not the word "END_DESC".

Label Enters the "Label" mode so that any LCC, IOC, INC or pin can be labeled. After a LCC or IOC is labeled, the equations related to the labeled cell are automatically generated in the source file (all equations equate to 0). The number and type (sum or product equations) of equations generated depends on the device type and the configuration of the cell (Table 11-2). **In PEEL Arrays, note that the equations are generated only if both the LCC and its associated IOC are previously unused or unlabeled.**

If the label for the LCC or IOC is deleted and its associated cell (IOC or LCC) is unused, then all the equations are automatically deleted.

Below is an example of the four equations generated for a labeled PA7024 LCC (assume the label is "ITEST").

Example:

<u>Configuration</u>	<u>Equations generated</u>
D-type flip-flop	!TEST.D = 0;
Async. Preset	!TEST.AP = 0;
Async. Reset	!TEST.AR = 0;
Assigned IOC is an I/O type	!TEST.OE = 0;

Assume that the flip-flop's output of the LCC is connected to the IOC.

<u>PEEL Device</u>	<u>Number of equations per IOC</u>
18CV8, 22CV8 20CG10A, 22CV10A/A+,	1 sum equation, 1 product equation
<u>PEEL Array</u>	<u>Number of equations per LCC/IOC pair</u>
PA7024, PA7128 PA7140	4 sum equations

Table 11-2. Number of Equations per IOC or LCC/IOC pair

Labeling Methods

Below are the three methods of labeling cells and pins.

1) **Click and Type method:**

This is the normal method of labeling the cells or pins. Move the mouse cursor and click the mouse button to select the cell or pin. Type in the label and press the ENTER key or right button of the mouse to complete the labeling procedure. Repeat this procedure for all cells and pins.

2) **Group (Set) method:**

The group or set method is designed for labeling a group of cells or pins with names that differ by a single alphabet character or a set of numbers. Some examples of the group names are: ModeA, ModeB, ModeC; AD0, AD1, ..., AD15; and A0, A1, ..., A12.

The first step in implementing this method is to click at a cell (IOC, INC, LCC or pin) which will be the starting cell, i.e. the first label in the group will be assigned to this cell. If the starting cell is an IOC, INC or pin, then the labels will be assigned to the next cell or pin **in ascending order**. For PEEL Arrays, if the starting cell is an LCC, then the labels will be assigned to the subsequent LCCs in ascending order (i.e., 1A, 2A, ..., 1B, 2B,...5D). After the starting cell has been selected, type the *group name* in the label window.

Format of the group name is:

```

prefix name  + [A..Z]  + suffix name
              + [Z..A]  +
              + [1..n]  +
              + [n..1]  + (where n > 1)
  
```

Some examples are:

Group Name	Assigned Labels
Q[0..3]	Q0, Q1, Q2, Q3
ADDR[9..13]	ADDR9, ADDR10, ADDR11, ADDR12, ADDR13
D[99..102]_IN	D99_IN, D100_IN, D101_IN, D102_IN
OUT[1000..998]	OUT1000, OUT999, OUT998
IN[51..49]DATA	IN51DATA, IN50DATA, IN49DATA, IN48DATA
[A..C]10	A10, B10, C10
![Z..X]1	!Z1, !Y1, !X1

3) **Keyboard method:**

Like the Group method, the keyboard method also allows labels to be assigned quickly. However, this method is more suitable for assigning labels which are significantly different from each other, i.e. they differ by more than two alphabet characters. Some of the label examples are INPUT, OUTPUT, ADDR1A, ADDR1B, OE, READ, !WRITE and etc. Normally to assign these labels you would need to implement the "Click and Type" method. But, performing this click and type task repeatedly for

twenty cells is a very tedious job. The "Keyboard" method shortcuts this task by bypassing the mouse click procedure.

In this method, you should first click on a cell (or pin) which you want the label to start from (defaults to the first pin if no pin or cell is selected). After typing in the label, press the [ENTER] key to implement the assignment (like in the "Click and Type" method). If the [ENTER] key is pressed the second time, the hand mouse cursor automatically advances to the next cell **in ascending order**. You can now type in the label for the current selected cell, and then press the [ENTER] key twice to advance to the next cell. Repeat the procedure until all the cells are labeled.

Please note that if you move your mouse cursor at any time during this mode, the "Keyboard" labeling will be aborted.



Note that all three methods of labeling cells and pins can be used in conjunction with each other. The "Click and Type" method can be used to select a new starting cell for the "Group" and "Keyboard" methods.

Renaming labels

The Label function can also be used for renaming the pins, IOCs, INCs or LCCs. During the renaming process, the previous labels used in the IOC, INC and LCC configuration, DEFINE, STATE_DIAGRAM, TRUTH_TABLE and EQUATIONS sections will automatically be replaced by the new label. This replacement process allows the user to change the pin or cell labels with ease so that the labels that are used throughout the PSF file need not be manually changed. An example of label replacement is:

	Before Change	After Change
Pin Label	TEST	/TEST1
Equations	OUT.COM = A & TEST	OUT.COM = A & TEST1
	OUT.OE = /TEST	OUT.OE = /TEST1

As seen in the previous example, the replacement process changes the label and the input signal active level. However, the logic of the equation remains unchanged. For instance, the OUT output which is controlled by the OUT.OE equation is enabled on a FALSE or OFF condition. With the TEST input the FALSE condition is a HIGH signal. On the other hand, the FALSE condition for the /TEST1 input is a LOW signal.

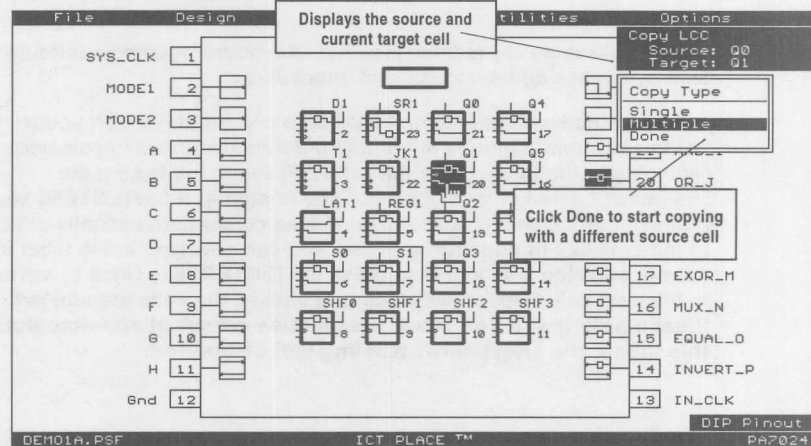


Figure 11-7. Copy Mode

- Copy** Copies the selected LCC's, IOC's or INC's configuration into another cell, but does not copy the equations. Select the "Multiple" option in the Copy Type window for doing multiple copying (Figure 11-7), i.e., copying from one cell into many cells. Select "Done" to complete the current "Multiple" copying set and start another. The only restriction in the "Copy" mode is that the source and target cells must be of the same type, i.e., LCC to LCC, IOC to IOC and INC to INC.
- Swap** This mode allows swapping of LCCs, IOCs, INCs or pins to reorganize your design. The functions of the cells do not change. There are two restrictions when swapping the two cells.
1. Both the source and target cells must be of the same type, i.e., LCC with another LCC, IOC with another IOC, and INC with another INC.
 2. For PEEL Arrays, the swapping of IOCs or LCCs are not permitted if the two global cell mode is used and if one of the following is true: a) the cells that are being swapped are IOCs which are located on the opposite sides of the pin block diagram; or b) the cells that are being swapped are LCCs which are connected to IOCs that are located on the opposite sides of the pin block diagram.
- Clear** Clears the LCC, IOC or INC. This sets a default configuration to the cells and renames the sum outputs according to the new configuration. After clearing both the LCC and its assigned IOC, all the sum equations associated with this cell are deleted.

Allocate Allocates the LCC or IOC for state-machine or truth table design. Before the cell can be used for allocation, it must first be labeled. This mode also allows a state-machine or truth table design to be created, deleted or modified. For state-machine design, the allocated cells will be surrounded by a border. For truth table design, the allocated cells will be indicated by "In" and "Tn" (inputs and outputs respectively), where n ranges from 1 to 10. Note that only the outputs of the truth table ("Tn") will be marked after exiting the "Allocate" mode. See Sections 11.10 and 11.11 for detailed descriptions of the state diagram and truth table designs.

Macro Displays the macro definitions in the PSF design file. Macro definitions are text statements which succeed the keyword "DEFINE" but precede one of the following reserved words: STATE_DIAGRAM; TRUTH_TABLE; or EQUATIONS.

Auxiliary Additional functions such as Security Bit, Signature and Zero-Power options which are found in the Peel Arrays and in some PEEL Devices. Below is a brief description of each function; refer to the ICT data book for more information.

Security Bit - Setting this feature ON enables the security bit to be programmed on the device (inserts the "G1" field in the JEDEC file). Once the security bit has been programmed, the design programmed into the device cannot be read back (except for the Signature Word). All PEEL products provide the security bit feature.

Signature Word - The Signature Word of the device allows a user ID to be stored in the device so that it can be read back for design verification even after the security bit has been programmed. Devices with the Signature Word (number of 8-bit bytes in parenthesis) are PA7024 (8 bytes), PA7140 (2 bytes), PA7128 (1 byte), PEEL22CV10A+ (3 bytes) and PEEL22CV10AZ+ (8 bytes).

Example: Signature = ABC [ENTER]

(Converts the characters A, B, C to the ASCII values 65, 66 and 67 respectively. Each character requires an 8-bit byte.)

Input and I/O Pin Pull-Up For the PEEL22CV8 only, this feature enables ("ON") or disables ("OFF") the pull-up circuitry on all input and I/O pins. The default setting is "OFF".

Clock Polarity - For PEEL22CV10AZ+ only, this feature allows clock polarity to be set. The default setting is "NON-INVERTED" which results in positive-edge clocking.

Setting the polarity to "INVERTED" will result in negative-edge clocking.

Clock Select - For the PEEL22CV10AZ+ only, this feature allows global clock selection between "PIN 1" (external) and "P-TERM" (internal product-term) clocks.

LCC Re-Assign.. (PEEL Arrays only) Allows the two internal and external outputs of the LCC to be separated and re-assigned. Below are the requirements for re-assigning the LCC.

- 1) The IOC's and LCC's of both source and target cells must be labeled.
- 2) The internal and external LCC outputs must not be sharing the same sum term, i.e., they must be from separate sum terms.
- 3) All sum terms must be used, i.e., the output equation extensions must not contain the ".SUMx" extension where $x = A..D$ for sums A through D.
- 4) The source and target LCCs must have the same configurations prior to the re-assignment. Use the "Copy" function to copy the configurations of the LCC (and possibly the IOC) from the source to the target cell. All LCCs and IOC's can be reconfigured later for your specific application requirements.

Example:

Figure 11-8 illustrates a typical example which requires the LCC re-assignment feature. In this example, a design modification is required to make the output "TESTOUT" synchronous with the clock "CK1". Currently, the output "TESTOUT" is a combinatorial output. This output would need to become registered in order to be synchronous with the clock "CK1". The problem is that the register in the LCC associated with this output is

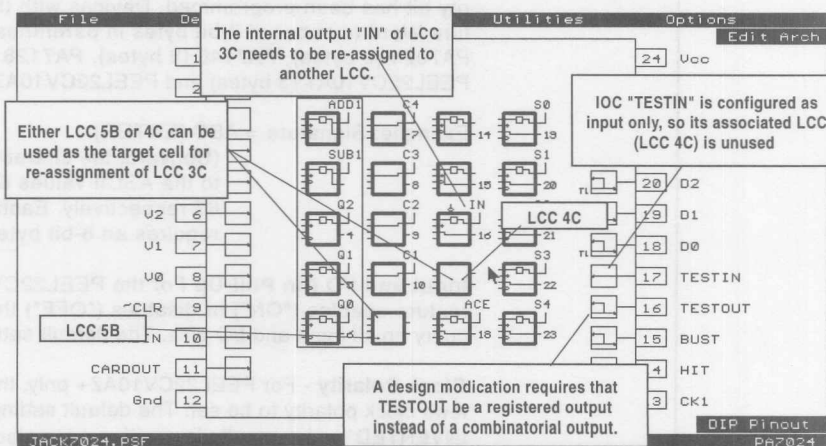


Figure 11-8. A typical example for re-assigning the LCC

already being used for another function. The internal output "IN" for the LCC 3C can be duplicated by copying the configuration of the LCC 3C into an empty LCC and re-typing the equations. However, a faster method is to use the "LCC Re-Assign" command which separates the output "IN" from the LCC 3C and re-assigns it to another IOC with an unused LCC (LCC 4C or 5B).

The procedure for re-assigning the internal output "IN" in LCC 3C is as follows:

- 1) Change the configuration of the LCC 3C and IOC "TESTIN" so that all the sum terms are used. In this example, set the IOC "TESTIN" to an I/O type instead of input only.
- 2) Label the target cell LCC "4C".
- 3) Copy the cell configurations, using the LCC 3C "IN" and IOC "TESTIN" as the source cells. The target cells will be the newly labeled LCC 4C and the IOC "TESTOUT".
- 4) Select the "LCC Re-Assign" command and click the source and target LCC (LCC 3C and 4C respectively).
- 5) Reconfigure all the cells (both source and target LCCs and IOCs) for their specific application requirements, i.e., IOC "TESTIN" to input only, IOC "TESTOUT" to output only, etc.

Global Toggles between the one or two global cell mode. If two global cells are used, swapping is not allowed with IOCs that are located on the left and right sides of the device, or with LCCs which are associated with IOCs that are located on the left and right sides of the device. This feature allows the device to be separated into two parts with each part containing its own high speed clock. Please refer to the ICT data book for more information on the benefits of the one and two global cell modes.

11.5 Design Operation - Pin Block Diagram Screen

The default function for the pin block diagram screen is the Edit Architecture mode (Edit Arch). This mode is automatically set when the PLACE software is initially entered. It allows selection of the Logic Control Cells (LCCs), I/O Cells (IOCs), Input Cells (INCs) or Global Cells (GBCs) for controlling cell configurations.

The PA7140 pin block diagram shown in Figure 11-9 illustrates the PLCC pinout configuration, which is the default for this device. Other devices, such as the PEEL22CV10A shown in Figure 11-10, default to the DIP configuration. The PLCC configuration can be set in the "Options" menu, refer to Section 11.13 for more information.

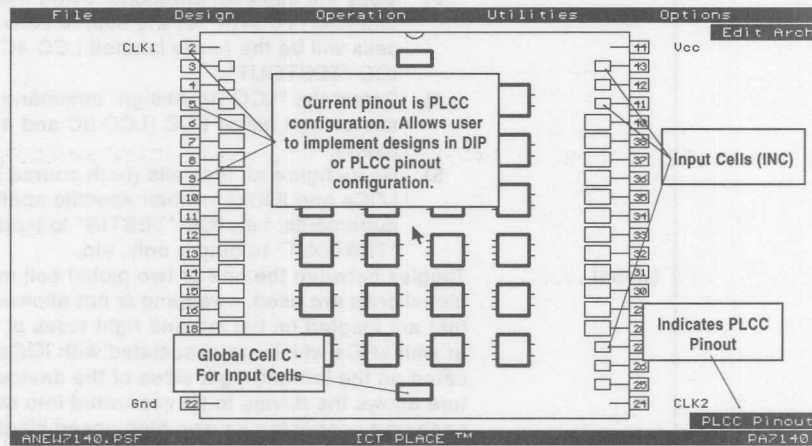


Figure 11-9. Pin Block Diagram of the PA7140

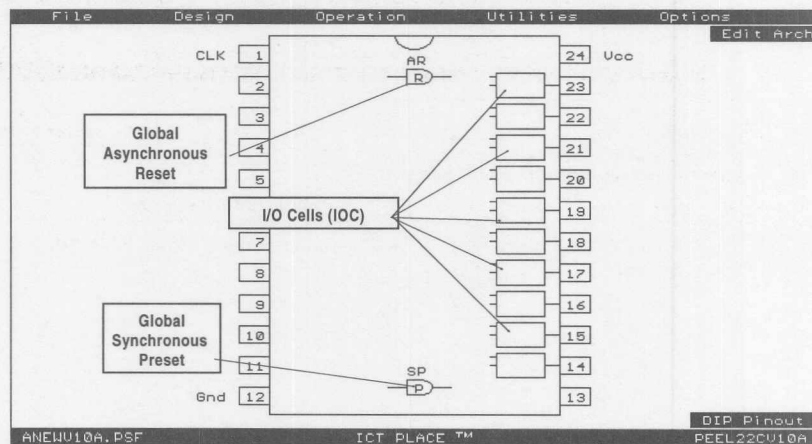


Figure 11-10. Pin Block Diagram of the PEEL22CV10A

11.6 Design Operation - LCC and IOC Screen

If a Logic Control Cell (LCC) or I/O Cell (IOC) is selected from the pin block diagram screen, the screen zooms into the selected cell for a close-up view of the cell configurations (Figure 11-12). Note that both the LCC and its currently connected IOC are displayed. In this screen, selections can be accomplished by moving the mouse cursor to the "selectors" such as the register's "rectangle", polarity "bubble", OR gates, or the "Smile Face" selectors. Except for the OR gate, all of the above selectors are highlighted when selected and are used for controlling the cell configurations.

Selecting any of the four OR gates will display its associated equation. Move the cursor inside the equation window and click to enter the text editor. Click-R to return from the editor, to complete the selected mode or function, or to return to the block diagram screen.

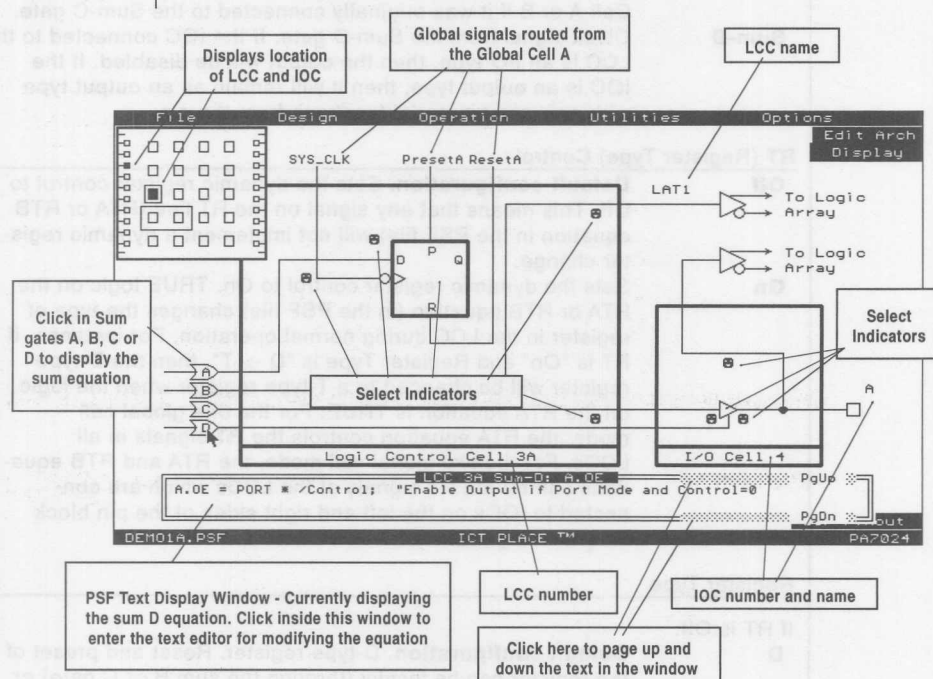


Figure 11-11. LCC and IOC screen of the PA7024

Select Indicators in PEEL Arrays (PA7024, PA7128 and PA7140)

Below are the descriptions of the "select indicators" found in all PEEL Arrays. Unless specified otherwise, all "select indicators" are applicable for all the PEEL Array devices.

Clk (Clock) Select

/Global	Inverted clock signal from the Global Cell A or B. If the two global cell mode is used, then LCCs connected to IOC's on the left and right sides of the pin block diagram are controlled by Global Cells A and B respectively. For one global cell mode, all global signals are routed from Global Cell A.
Global	Default configuration. Non-inverted clock signal from the Global Cell A or B.
Sum-C	Clock signal from the Sum-C gate. The Reset signal for the LCC register will automatically be routed from the Global Cell A or B if it was originally connected to the Sum-C gate.
Sum-D	Clock signal from the Sum-D gate. If the IOC connected to the LCC is an I/O type, then the output will be disabled. If the IOC is an output type, then it will remain as an output type with only combinatorial feedback from the pin.

RT (Register Type) Control

Off	Default configuration. Sets the dynamic register control to Off. This means that any signal on the RT line (RTA or RTB equation in the PSF file) will not implement a dynamic register change.
On	Sets the dynamic register control to On. TRUE logic on the RTA or RTB equation (in the PSF file) changes the type of register in the LCC during normal operation. For instance, if RT is "On" and Register Type is "D -> T", then the D-type register will be changed to a T-type register when the logic on the RTA equation is TRUE. For the one global cell mode, the RTA equation controls the RT signals in all LCCs. For the two global cell mode, the RTA and RTB equations control the RT signals of the LCCs which are connected to IOC's on the left and right sides of the pin block diagram respectively.

Register Type

If RT is Off:

D	Default configuration. D-type register. Reset and preset of the register can be locally (through the sum B or C gate) or globally (ResetA or PresetA equation) controlled.
T	T-type register. Reset and preset of the register can be locally (through the sum B or C gate) or globally (ResetA or PresetA equation) controlled.
JK	JK register. Sum-A for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset.

If RT is On:

D -> T	Default configuration. D-type register when the RT signal is FALSE, and T-type register when it is TRUE. Reset and preset can be locally or globally controlled.
D -> JK	D-type register when the RT signal is FALSE, and JK-type register when it is TRUE. For the JK-type register, Sum-A is used for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset.
T -> D	T-type register when the RT signal is FALSE, and D-type register when it is TRUE. Reset and preset can be locally or globally controlled.
JK -> D	JK-type register when the RT signal is FALSE, and D-type register when it is TRUE. For the JK-type register, Sum-A is used for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset.



Note that the Sum-B gate cannot be used for both K-input and preset for the register.

Preset and Reset for the LCC Register

The output of the LCC register is set to a HIGH signal when the preset signal is TRUE. On the other hand, the output of the register goes LOW if the reset signal is TRUE. **If both the preset and reset signals are TRUE, then the preset signal takes precedence over the reset signal.**

There is no dedicated MUX for controlling the preset or reset of the LCC register. Both of these signals are indirectly controlled by the "Clk Select", "Register Type", "Buried Output" and "Ext Output" selections. **The same Sum (OR) gate allocated for any of the above configurations cannot be used for presetting or resetting the LCC register.** So, the PLACE software automatically switches the preset or reset to the global signal when the local sum gate is used.

Buried Output (Internal Output of the LCC)

Reg-Q	Default configuration. Connects the output of the LCC register to the internal or buried output of the LCC.
Sum-A	Connects the Sum-A gate to the internal or buried output of the LCC.
Sum-B	Connects the Sum-B gate to the internal or buried output of the LCC. If the preset of the register is locally controlled (through Sum-B), it will automatically be set to global preset.
Sum-C	Connects the Sum-C gate to the internal or buried output of the LCC. If the reset of the register is locally controlled (through Sum-C), it will automatically be set to global preset.

Ext Output (External Output of the LCC to the IOC)

Reg-Q	Default configuration. Connects the output of the LCC register to the external output of the LCC.
Sum-A	Connects the Sum-A gate to the external output of the LCC.

Sum-B	Connects the Sum-B gate to the external output of the LCC. If the preset of the register is locally controlled (through Sum-B), it will automatically be set to global preset.
Sum-C	Connects the Sum-C gate to the external output of the LCC. If the reset of the register is locally controlled (through Sum-C), it will automatically be set to global preset.

OE (Output Enable) Select

I/O	Default configuration. Sets the IOC to I/O type. Sum-D is used for the output enable control. If the LCC Clk Select is set to Sum-D, the IOC changes from I/O to input type automatically.
Input	Sets the IOC to input type. If Sum-D is not used for the LCC clock, then it will be disabled.
Output	Sets the IOC to output type. If Sum-D is used for the LCC clock, then the Feedback Type will automatically be set to combinatorial.

Feedback Type

In the normal configuration, whether the IOC is an I/O, input or output type, this multiplexer controls the path from the pin. However, in the PA7128 and PA7140 devices, the option "FB Mux" allows the path to come from the Sum-D gate.

Com	Default configuration. Combinatorial path from the pin or Sum-D.
Reg	Registered path from the pin or Sum-D. The clock for the register can be directly from the CLK1 or CLK2 pin, or PCLK product term.
Lat	Latched path from the pin or Sum-D. The latch trigger can come directly from the CLK1 or CLK2 pin, or PCLK product term.

Out (Output) Polarity

Invert	Inverts the output to the pin for active Low output.
Non-invert	Default configuration. Non-inverted output for active High output.

FB Mux (PA7128 and PA7140 only)

Pin	Default configuration. Sets the feedback path to come from the pin.
Sum-D	Sets the feedback path to come from the Sum-D gate. With this configuration, the IOC automatically becomes an output pin with no feedback from the pin. Therefore, the Sum-D signal will be buried. See Figure 11-12.

Select Indicators in the PEEL Devices

Output Select	
Com	Default configuration. Sets the IOC to combinatorial output. In the 22CV10A devices, the feedback path is automatically set to come from the pin with this configuration. For other devices such as PEEL18CV8, the feedback path is controlled by the "Feedback Type" MUX.
Reg	Sets the IOC to registered output. In the 22CV10A devices, the feedback path is automatically set to come from the \bar{Q} of the register with this configuration. See Figure 11-13. The register is triggered on the rising-edge of the clock.

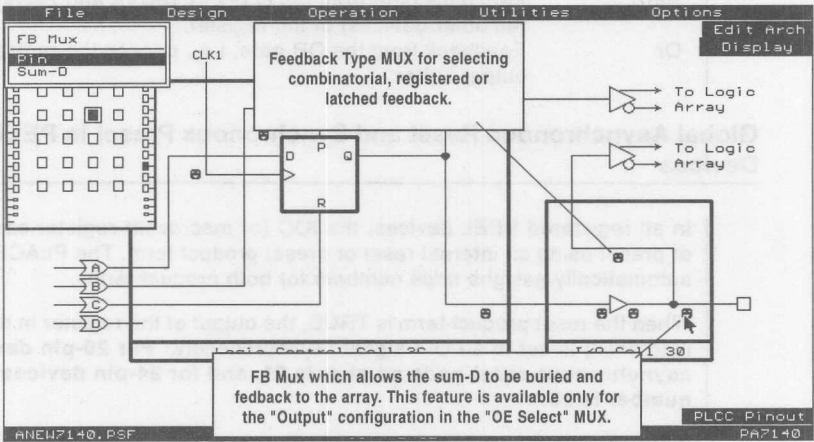


Figure 11-12. LCC and IOC screen of the PA7140

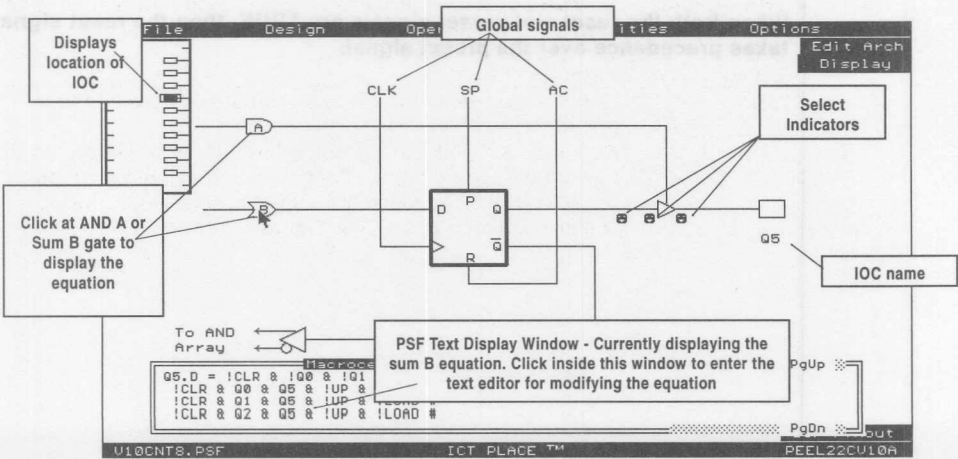


Figure 11-13. IOC screen of the PEEL22CV10A

OE (Output Enable) Select

I/O	Default configuration. Sets the IOC to I/O type. Depending on the device, a sum or product term controls the output enable term.
Output Enabled	Enables the output in the IOC.
Output Disabled	Disables the output in the IOC.

Out (Output) Polarity

Invert	Default configuration. Inverts the output to get an active Low output.
Non-invert	Buffers the active High output.

Feedback Select (18CV8, 22CV8, 20CG10A, 22CV10AZ+ and 22CV10A+)

Pin	Feedback path from the pin.
Reg	Feedback path from the Q (PEEL18CV8 and 22CV8) or \bar{Q} (all other devices) of the register.
Or	Feedback from the OR gate, i.e., prior to the register and output buffer.

Global Asynchronous Reset and Synchronous Preset in PEEL Devices

In all registered PEEL devices, the IOC (or macrocell) register can be reset or preset using an internal reset or preset product term. The PLACE software automatically assigns node numbers for both product terms.

When the reset product term is TRUE, the output of the register in the IOC (or macrocell) is set to a LOW signal asynchronously. **For 20-pin devices, the asynchronous reset node number is 21, and for 24-pin devices the node number is 25.**

When the preset product term is TRUE, the output of the register in the IOC changes to a HIGH signal (synchronously) with the rising-edge of the clock signal. **The node number for the preset product term is 22 and 26 for the 20 and 24-pin devices respectively.**

When both the reset and preset signals are TRUE, then the reset signal takes precedence over the preset signal.

11.7 Design Operation - Input Cell (INC) for PA7128 and PA7140

In addition to the IOCs and LCCs, the PA7128 and PA7140 have Input Cells (INCs). Each INC allows the input to be configured as combinatorial, registered or latched input (Figure 11-14).

Input Type

Com

Default configuration. Sets the input to be combinatorial.

Reg

Sets the input to be registered. The clock for the register is controlled by the Global Cell C.

Lat

Sets the input to be latched. The trigger for the latch is controlled by the Global Cell C.

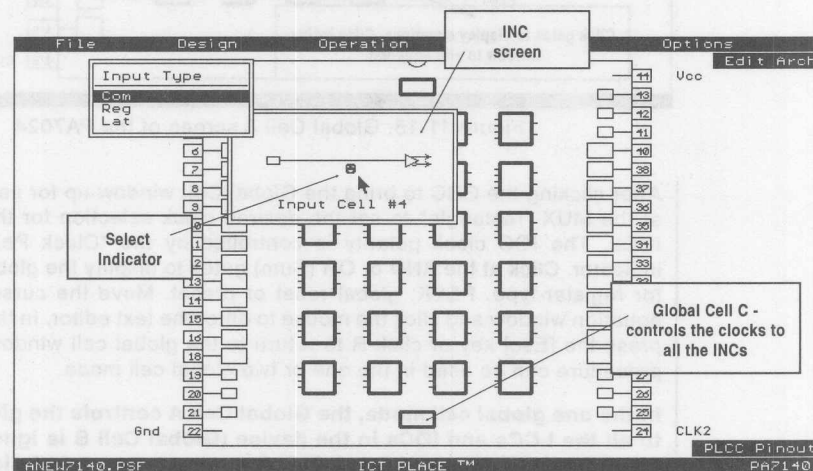


Figure 11-14. INC screen of the PA7140

11.8 Design Operation - Global Cell (GBC) for PEEL Arrays

Global Cells A and B

In PEEL Arrays, the Global Cells (GBCs) A and B which are located at the top of the pin block diagram are used to control the global signals for the LCC and IOC. See Figure 11-15. These global signals include the clock for the LCC and IOC, and preset, reset and register type control for the LCC.

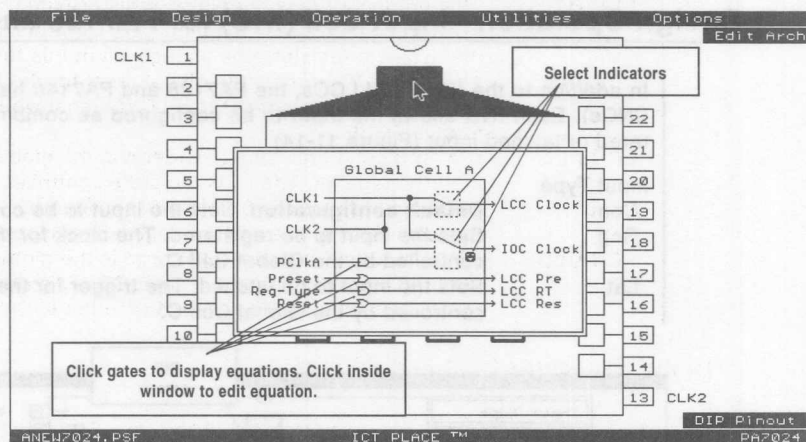


Figure 11-15. Global Cell A screen of the PA7024

After clicking the GBC to bring the Global Cell window up for selection, click at the MUX "rectangle" to set the desired clock selection for the LCCs and IOCs. The IOC clock polarity is controlled by the "Clock Polarity" select indicator. Click at the AND or OR (Sum) gates to display the global equations for register-type, PCLK, global reset or preset. Move the cursor inside the equation window and click the mouse to enter the text editor. In the text editor, press the [Esc] key or click-R to return to the global cell window. The same procedure can be used in the one or two global cell mode.

In the one global cell mode, the Global Cell A controls the global signals to all the LCCs and IOCs in the device (Global Cell B is ignored). In the two global cell mode, Global Cell A controls the global signals to the LCCs and its associated IOCs that are located on the left side of the pin block diagram. Global Cell B controls the global signals to the remaining LCCs and IOCs which are located on the right side of the pin block diagram.

Global Signals

LCC Clock	This signal clocks the register in the LCCs. The signal comes from one of the two dedicated clock pins, CLK1 or CLK2.
IOC Clock	This signal clocks the register in the IOCs. In addition to the two dedicated clock pins CLK1 and CLK2, the signal can come from a product term PCLKA (GBC A) or PCLKB (GBC B). The select indicator "Clock Polarity" allows the IOC clock polarity to be changed. The default configuration is "Pos" which means that the IOC register or latch is triggered on the rising-edge or HIGH signal. If the configuration is set to "Neg", then the register or latch is triggered on the falling-edge or LOW signal.
LCC Pre	This sum (OR) term is the global preset for the LCC register. The LCC register is preset to a HIGH signal when this sum term is TRUE. This term takes precedence over the reset term for the LCC register.

LCC RT	This product term is the global register-type change for the LCC. Each LCC has the option ("RT Control") of enabling the dynamic register-type change when this term is TRUE.
LCC Res	This sum (OR) term is the global reset for the LCC register. The LCC register is reset to a LOW signal when this sum term is TRUE.
LCC PLD	(PA7140 only) This sum (OR) term is the global preload for the LCC register. The LCC registers controlled by this global cell are loaded from the associated IOC pin when this sum term is true and the registers is clocked.
LCC ULD	(PA7140 only) This sum (OR) term is the global unload for the LCC register. The content of the LCC registers controlled by the global cell will be unloaded to the IOC pin when true.

Global Cell C (PA7128 and PA7140 only)

In addition to Global Cells A and B, the PA7128 and PA7140 have Global Cell C. This cell which is located at the bottom of the pin block diagram controls the global clock signal for the Input Cells (INCs). See Figure 11-16.

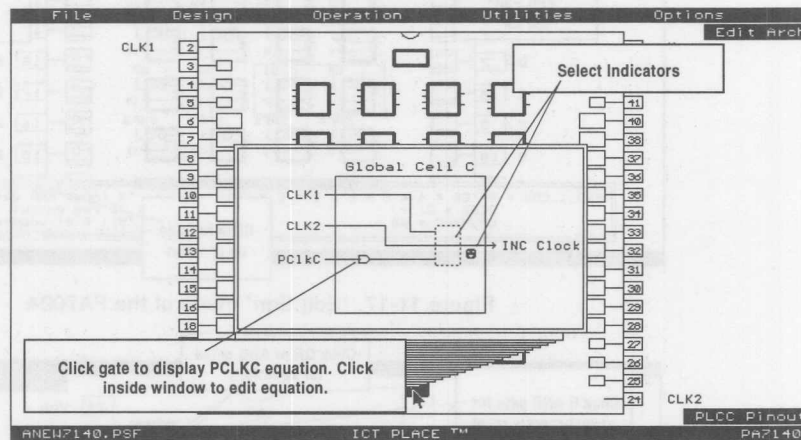


Figure 11-16. Global Cell C screen of the PA7140

11.9 Design Operation - Entering Equations

One of the primary methods of entering the design equations is via the "Edit Equation" mode which was discussed in Section 11.4. Figures 11-17 and 11-18 show the "Edit Equation" mode for the PA7024 and PEEL22CV10A devices respectively. In addition to the "Edit Equation" mode, equations can also be edited via the LCC and IOC screen (or just the IOC screen for the PEEL devices). Refer to Figures 11-19 and 11-20.

For editing equations for the global signals in the PEEL Arrays, please refer to Section 11.8 on "Global Cells for PEEL Arrays".

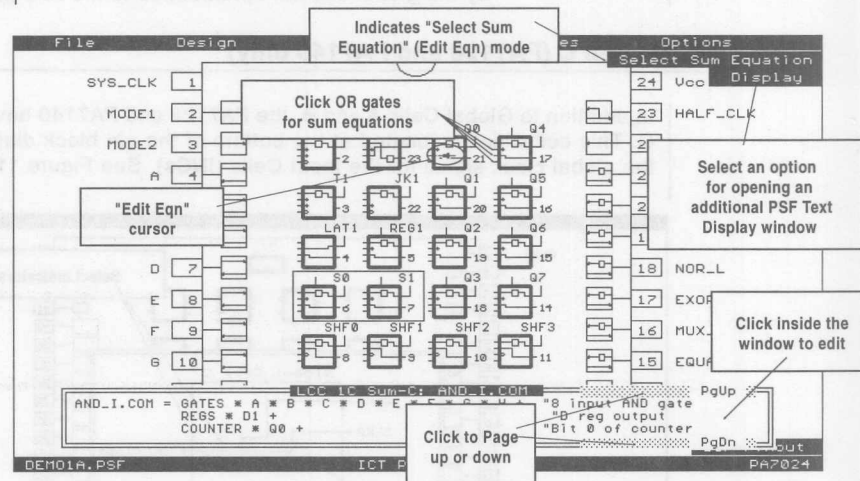


Figure 11-17. "Edit Eqn" mode of the PA7024

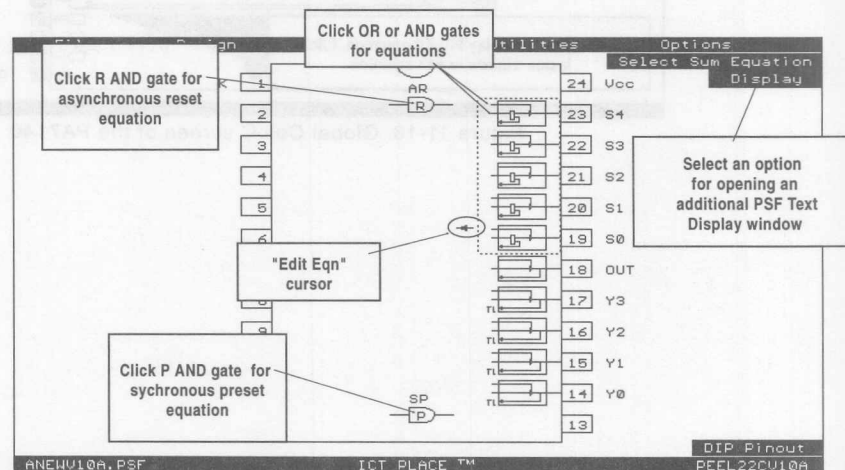


Figure 11-18. "Edit Eqn" mode of the PEEL22CV10A

After the cell (LCC or IOC) is labeled using the "Label" command in the "Design" menu window, the PLACE software automatically generates the equations. To edit or modify these equations, first, click at the desired OR (sum) or AND (product) gate to bring the equations into the PSF Text Display window (Section 11.12). Then, click inside the window to enter the text editor. When you are done editing the equations, press the [Esc] key or click-R to return to the previous screen. Whether the device is a PA7024, PEEL22CV10A or any other device, the procedure for entering the design equations remains the same.

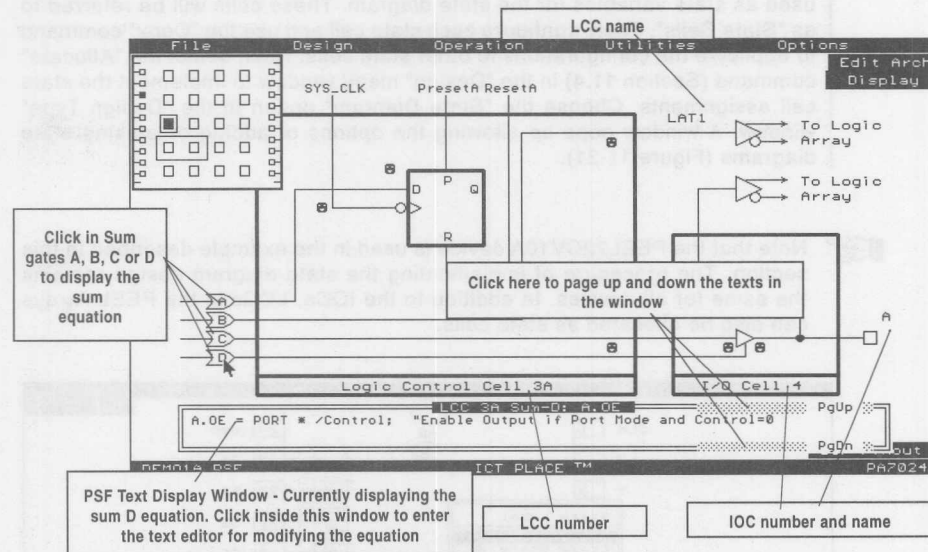


Figure 11-19. Editing equations in the LCC and IOC screen of the PA7024

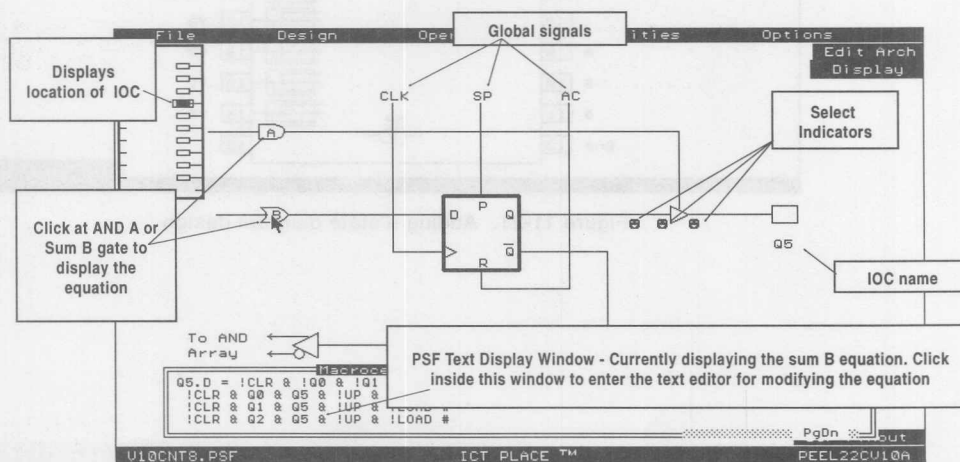


Figure 11-20. Editing equations in the IOC screen of the PEEL22CV10A

11.10 Design Operation - State Diagram Designs

An alternate method of describing a logic design is the state diagram design implementation. In this section, the procedure to implement the state diagram designs is discussed. The syntax for these state diagram designs are discussed in detail in Chapter 12 on "PLACE Design Language".

The first step in the state diagram design method is to label the cells to be used as state variables for the state diagram. These cells will be referred to as "State Cells". Then, configure each state cell and use the "Copy" command to duplicate the configurations to other state cells. Next, select the "Allocate" command (Section 11.4) in the "Design" menu window to implement the state cell assignments. Choose the "State Diagram" option in the "Design Type" window. A window pops up allowing the options of adding or erasing state diagrams (Figure 11-21).



Note that the PEEL22CV10A device is used in the example described in this section. The procedure of implementing the state diagram design remains the same for all devices. In addition to the IOCs, LCCs in the PEEL Arrays can also be allocated as state cells.

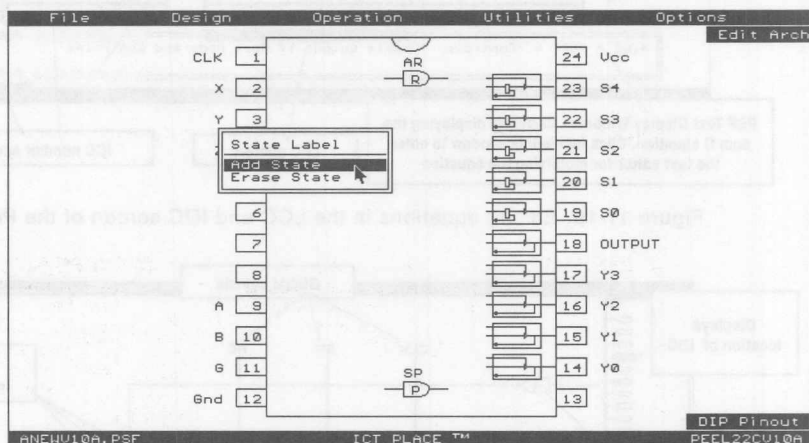


Figure 11-21. Adding a state diagram design

Type in the label for the new state diagram. The syntax of the label is similar to those used for labeling pins or cells (refer to Chapter 12 on "PLACE Design Language"). The next step is to allocate the state cells as illustrated in Figure 11-22.

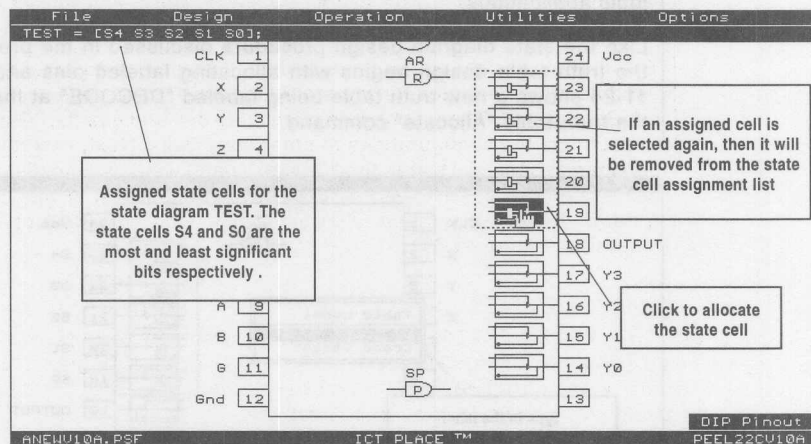


Figure 11-22. Allocating state cells for a state-diagram design

After completing the state cell assignments (by pressing the [Esc] key or click-R), a border surrounds the assigned state cells to indicate the state diagram. See Figure 11-23. Additional state diagrams are differentiated by the line types in the borders.

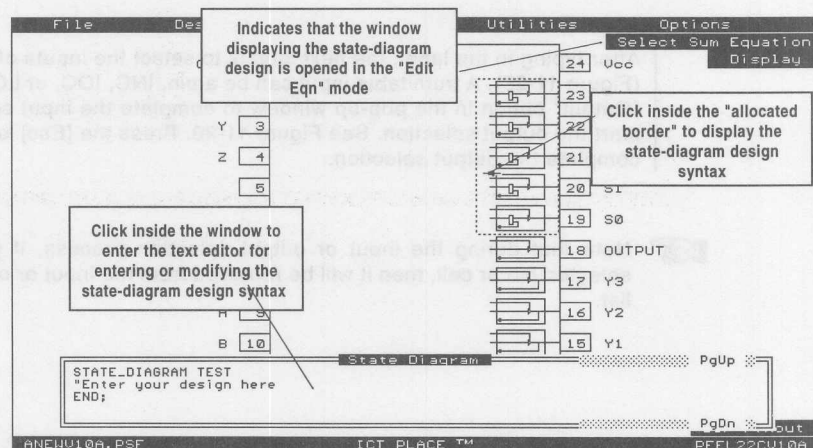


Figure 11-23. Entering design description for the state-diagram

11.11 Design Operation - Truth Table Designs

In truth table designs, the description of the logic design is in the form of a truth table. This design method is most suitable for random combinatorial logic applications.

Like the state diagram design procedure discussed in the previous section, the truth table design begins with allocating labeled pins and cells. Figure 11-24 shows a new truth table being labeled "DECODE" at the beginning of the truth table "Allocate" command.

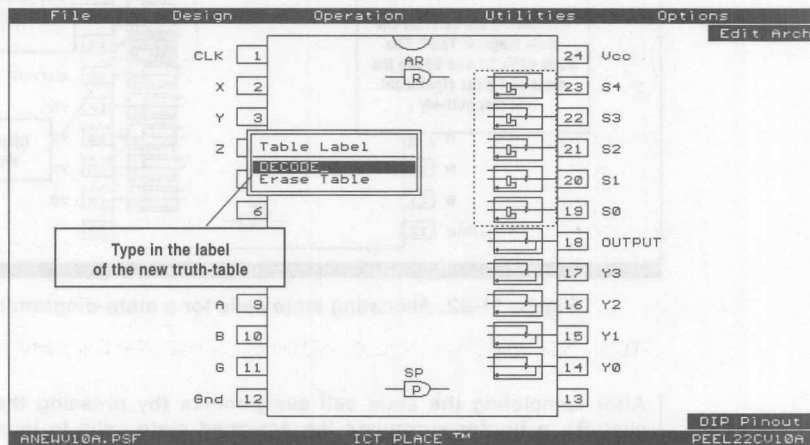


Figure 11-24. Entering the label for a new truth-table design

After typing in the label, the next step is to select the inputs of the truth table (Figure 11-25). A truth table input can be a pin, INC, IOC, or LCC. Click at the "Output" option in the pop-up window to complete the input selection and to start the output selection. See Figure 11-26. Press the [Esc] key or click-R to complete the output selection.



Note that during the input or output selection process, if you click on a selected pin or cell, then it will be removed from the input or output selection list.



Press the [Esc] key or click-R during the input or output selection process to abort or complete the "Allocate" command. A window will pop up to confirm implementing the changes made. Pressing the [Esc] key or clicking-R when the "Implement changes?" window is popped up will return you to the previous mode (input or output selection).

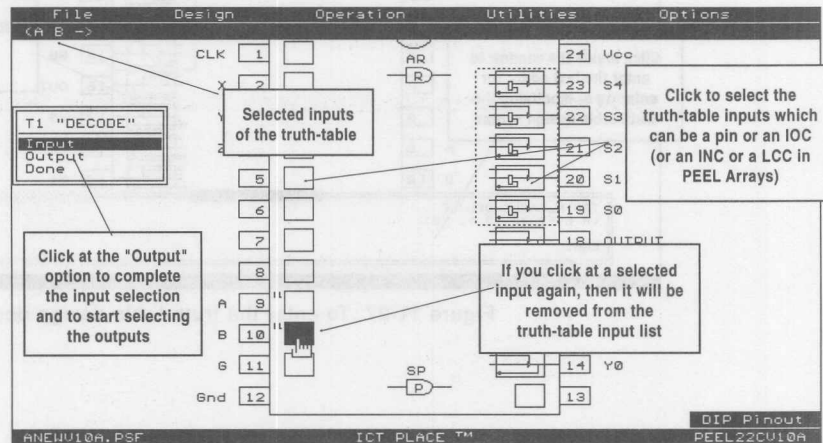


Figure 11-25. Selecting truth-table inputs

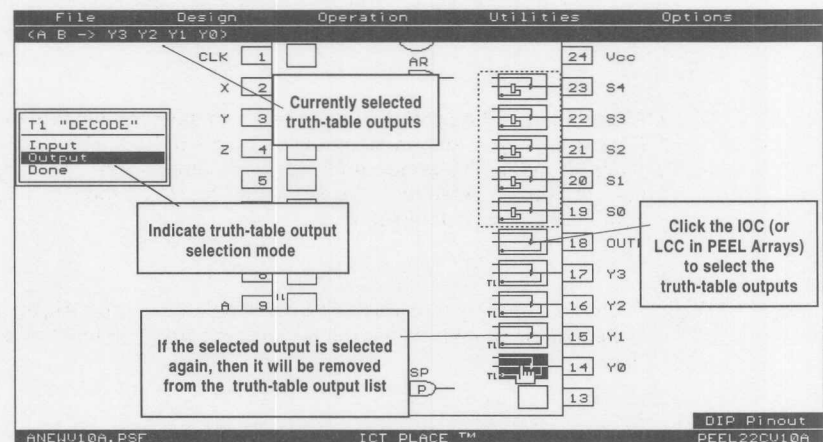


Figure 11-26. Selecting truth-table outputs

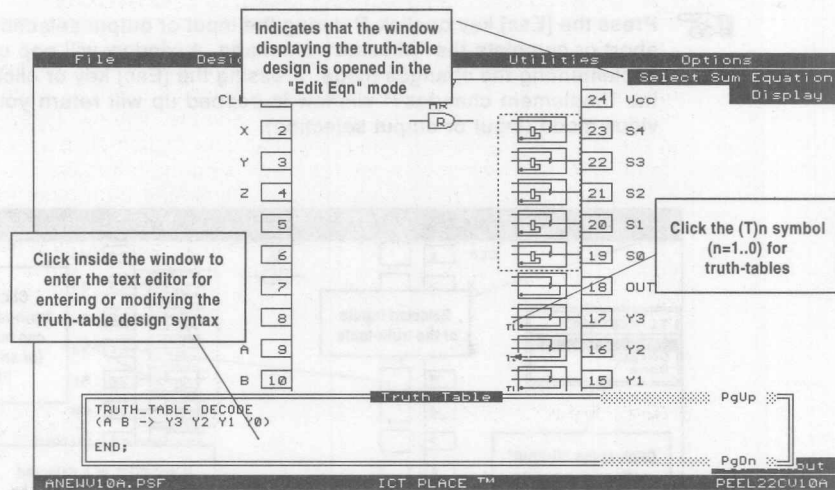


Figure 11-27. To enter the truth-table design description



Figure 11-27 shows the truth table window for entering the truth table design syntax. For more information on the syntax of the truth table design description, please refer to Chapter 12 on "PLACE Design Language".

11.12 Design Operation - PSF Text Display Window

The PSF Text Display Windows are the windows which can be opened to display the logic description of the current design, such as equations, state diagrams, truth tables, macro definitions, and etc. The two types of windows in the PLACE software are the Equation and Option Display windows. An Equation Display window is opened by clicking the left mouse button on any SUM or AND node (gate), state diagram block and truth table marker (indicated by Tn where n = 1 to 10). This window is always located at the bottom of the screen. Refer to Figures 11-28 through 11-30. On the other hand, the Option Display window is located at the top of the screen and is opened from the "Display" menu. The "Display" menu is selectable in the "Edit Equation" mode, LCC/IOC screen for the PEEL Arrays, and IOC screen for PEEL Devices. See Figures 11-28 and 11-29.

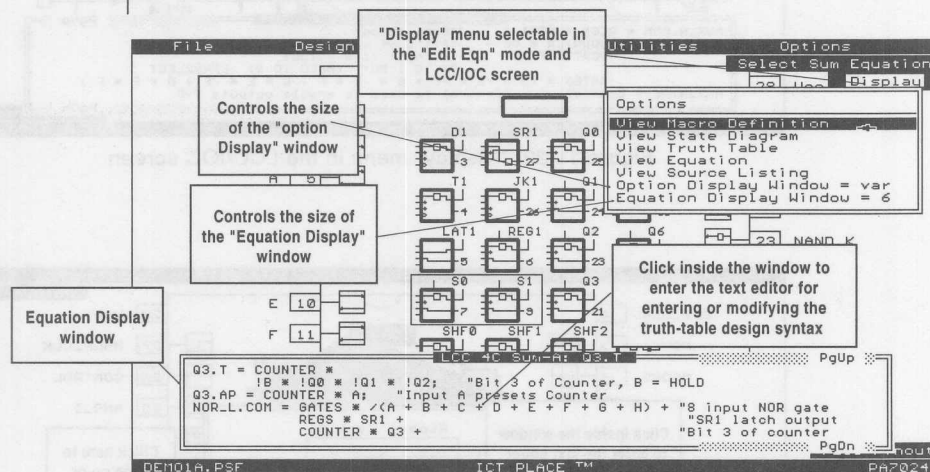


Figure 11-28. "Display" menu in "Edit Eqn" mode

Display Options

In the "Display" menu, there are several categories of the PSF design file which can be selected for viewing. The list includes Macro Definition, State Diagram, Truth table, Equation and Source File. With or without the Equation Display window opened, you can open this additional window by clicking on the selected category (Figure 11-31).



If the "Equation" or "Source File" option is selected, the window opens by displaying the most recently displayed page. This means that if you have previously opened the "Equation" or "Source File" window and have paged up or down, then the next time you select the same option the previous page will be displayed.

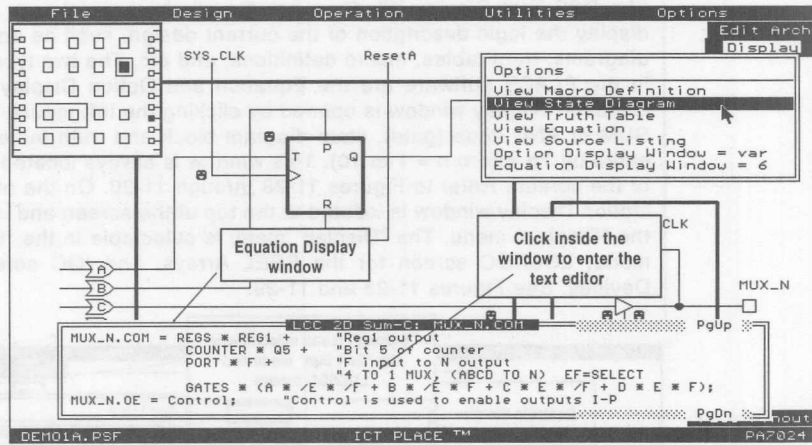


Figure 11-29. "Display" menu in the LCC/IOC screen

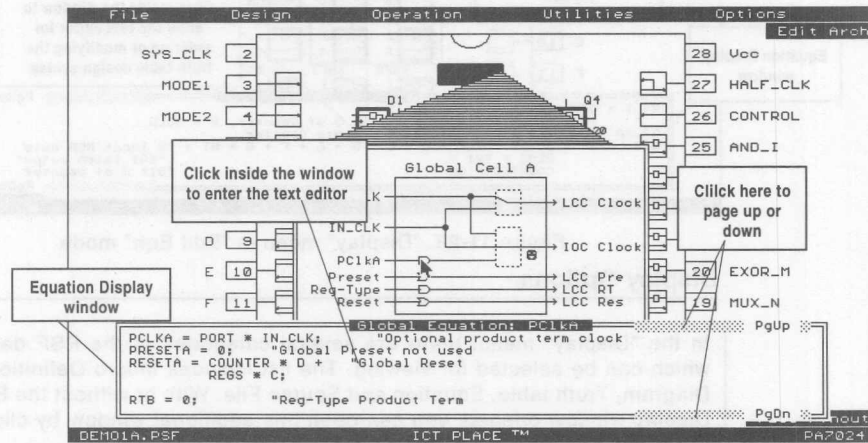


Figure 11-30. Equation Display window of the Global Cell A

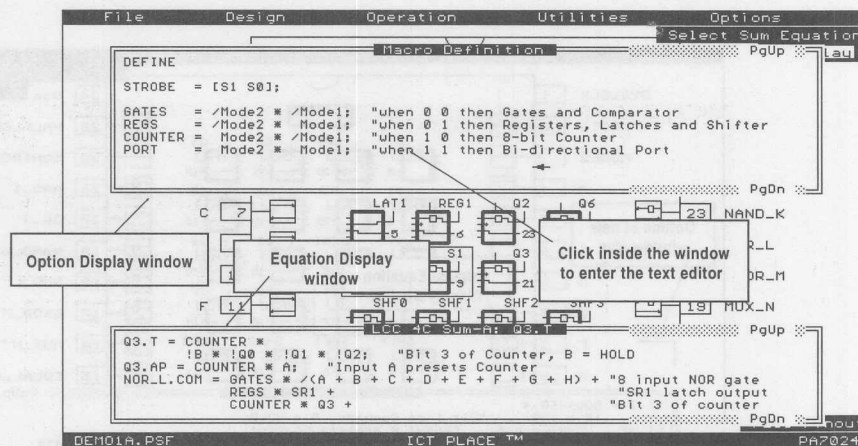


Figure 11-31. Both Equation and Option Display windows opened

Sizing the Display Windows

There are two ways in which you can size the display windows (Figure 11-32):

- ❑ The first method is by pressing the Up and Down cursor keys followed by the [Enter] key when the window is displayed. The first cursor key pressed enters the sizing mode by outlining the current window. Each subsequent cursor key moves the window border up or down. Then, press the [Enter] key to accept the selected size. The maximum number of lines for each window is 19.
- ❑ The second method is to use the last two options in the "Display" menu (Figure 11-28). Click at either option to advance the number of lines for the window. This number will be used the next time the window is opened. In addition, the selection "var" ("variable") is available for both these options. This selection (illustrated by "Option Display Window = var" or "Equation Display Window = var") allows the size of the window to be dependent on the type of design syntax selected. The criteria for setting the "var" window size are:
 - **Equations (Equation Display Window only):**
A set of equations will be displayed. The equations start from the selected SUM or AND gate label (e.g., Q1.D) and end with any of the following characters (in prioritized order): ";", "=", "TEST_VECTORS" or ASCII# 26 (End-of-File) character.
 - **State Diagrams:**
A state diagram design group which begins and ends with the keywords "STATE_DIAGRAM *statename*" and "END;" respectively.
 - **Truth Tables:**
A truth table design group which begins and ends with the keywords "TRUTH_TABLE" and "END;" respectively.
 - **Macro Definitions:** The displayed text will succeed the keyword "DEFINE" but precede "STATE_DIAGRAM *statename*", "TRUTH_TABLE" or "EQUATIONS".

For the "Equations" and "Source File" options in the Options menu, the "var" selection sets the window size to 19 lines (maximum number).

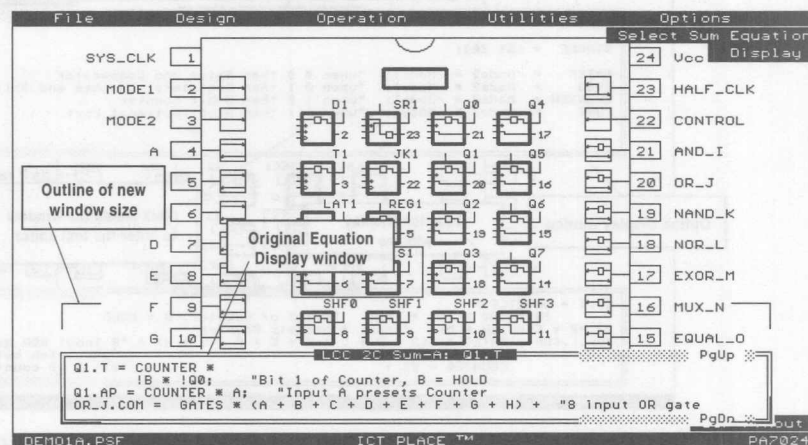


Figure 11-32. Sizing the Equation Display window

Paging Up and Down

The contents of the window can be paged up and down by pressing the PgUp and PgDn keys respectively. Paging up and down can also be accomplished by clicking at the PgUp and PgDn markers in the upper and lower right corner of the window (Figure 11-30).

Entering the PLACE Text Editor via the Display Window

Clicking the left button of the mouse within the Equation or Option Display window opens the PLACE text editor for entering or modifying the design syntax. In addition, the PLACE text editor highlights the selected block and moves the text cursor to the top of the block. The block that is highlighted depends on which Display Window the text editor was opened from. If the editor was opened via the Equation Display Window, then the equation, state diagram or truth table block will be highlighted depending on which design type was selected. If the Option Display Window was used instead, then the block displayed on the window will be highlighted in the text editor. To return to the previous screen, press the [Esc] key.

11.13 Design Operation - Options Menu

Set Pinout to DIP/PLCC Allows the pin numbers in the pin block diagram and LCC/IOC screen to show the pinout of DIP or PLCC package type. Figures 11-33 and 11-34 show the pinouts for DIP and PLCC packages respectively. **The default is the DIP pinout for all devices with the exception of the PA7140 device which defaults to the PLCC pinout configuration.** The pinout for the SOIC package is the same as the DIP package.

PLCC Configuration . . . Displays the design in the actual PLCC package form (Figure 11-35). Press the [Esc] key or click-R to return to the previous screen.

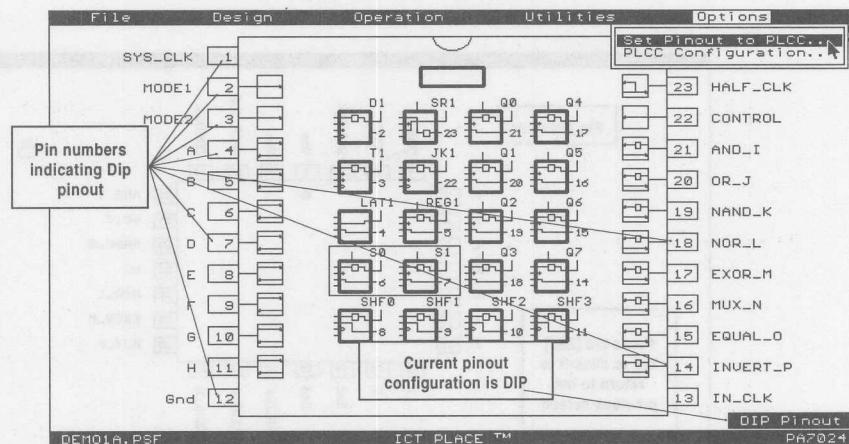


Figure 11-33. "Options" menu and DIP pinout for the PA7024

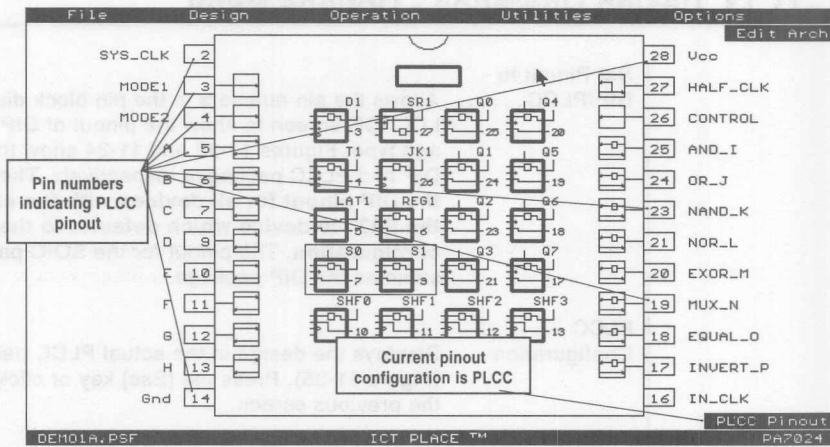


Figure 11-34. PLCC pinout for the PA7024

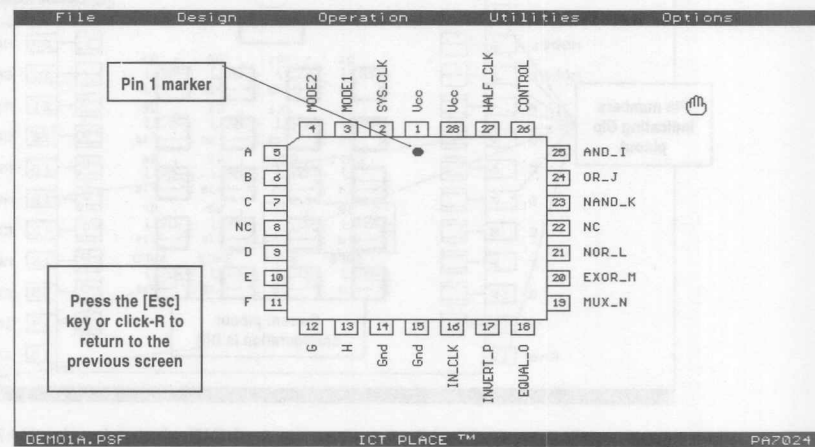


Figure 11-35. PLCC package configuration for the PA7024

11.14 Compile Operation - Main Screen

There are three windows in the main screen of the Compile Operation (Figure 11-36). Each of these windows provides a specific function for the compilation of PLACE Source Files (PSF).

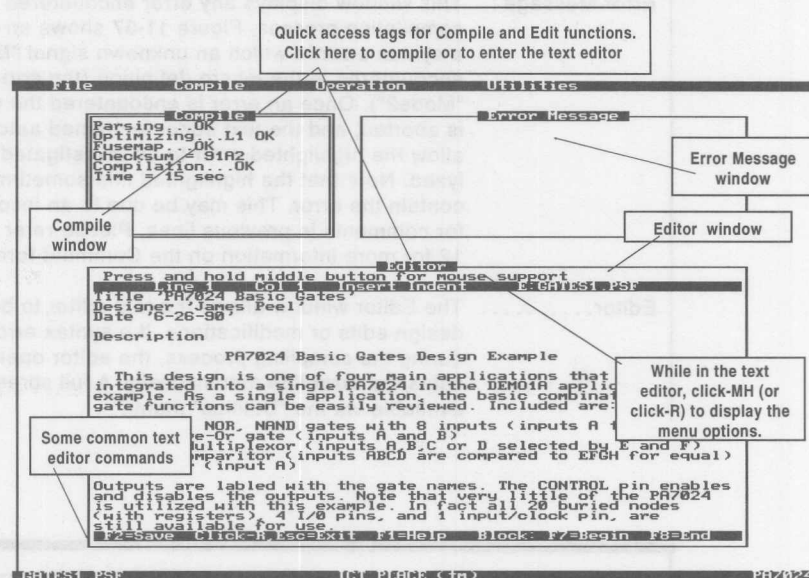


Figure 11-36. Compile Operation screen

Compile This window displays information regarding the status of the compilation. The compilation of a PSF file is a three step process: Parsing, Optimizing, and Fuse-mapping.

Parsing - Checks the syntax of the PSF file and displays the error in the Error Message window.

Optimizing - Implements logic transformation (converting complex equations into sum-of-product form) and reduction to the parsed PSF file, and outputs the results to a file with extension ".RED". The RED file is in the PSF format, hence it can be read into the Design Operation for analysis of the reduced equations. After optimization is completed, the reduction level implemented is displayed. For instance in Figure 11-36, the "L1" term in "Optimizing ...L1 OK" indicates that the reduction level L1 was used for the GATES1.PSF design, and the optimization process was successful (as indicated by the "OK").

Fuse-mapping - This is the final step in the compilation process. After successful optimization, the reduced equations are mapped into the device and a JEDEC programming file is created. In addition, the fuse-mapper creates

a ".MAP" file which contains information on how each equation is mapped in the JEDEC file.

Once the compilation is completed and successful, the checksum of the JEDEC file and compilation time will be displayed.

Error Message .. This window displays any error encountered during the compilation process. Figure 11-37 shows an example of a syntax error in which an unknown signal "MØDE2" was encountered in the macro definition (the correct signal is "Mode2"). Once an error is encountered the compilation is aborted, and the text editor is opened automatically to allow the highlighted error to be investigated or analyzed. Note that the highlighted line sometimes does not contain the error. This may be due to an incorrect format for comments in previous lines. Please refer to Chapter 12 for more information on the Comment format.

Editor..... The Editor window allows the text editor to be opened for design edits or modifications. If a syntax error is found during the compiling process, the editor opens and highlights the error line automatically. A full screen editor is available via the "Utilities" menu.

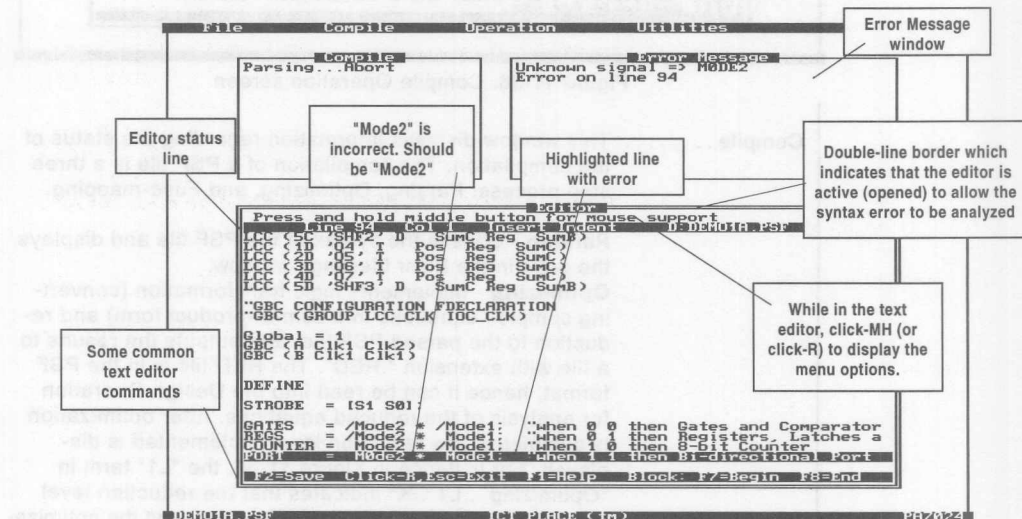


Figure 11-37. Encountering a compilation syntax error

11.15 Compiler Operation - Compile Menu

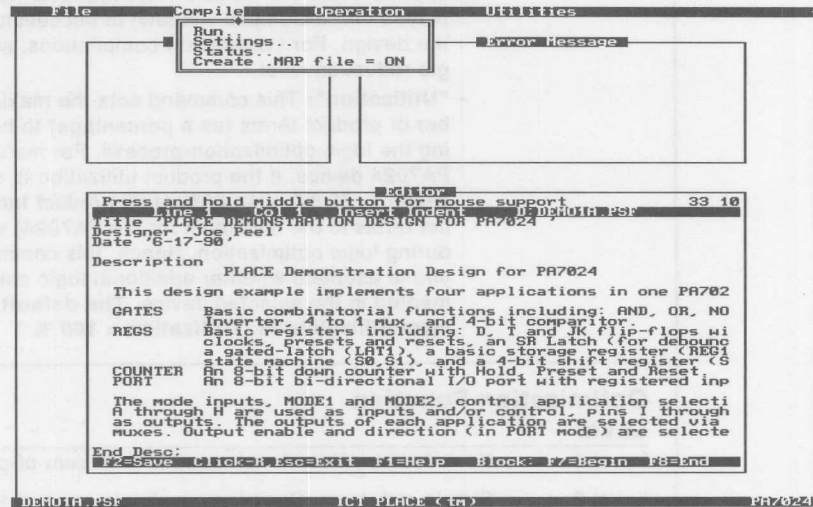


Figure 11-38. Compile menu

- Run.....** Compiles the currently selected PSF design file. If the compilation process is successful, then a JEDEC ".JED" file will be created. If a compilation error occurs, an error message will be displayed in the Error Message window. In addition, the editor will be opened and the line containing the error highlighted automatically. You can then make the edits here or go back to the Design operation to correct the source file. Please refer back to Section 11.14 for more information on the compilation process.
- Note:** The compiler can be executed by clicking on the "Compile" window heading.
- Settings.....** Allows the selection of logic optimization level and product term utilization as listed in Table 11-3.
- **The default option for the reduction level selection is "Auto 1-5".** The "Auto" reduction levels refer to the automatic increments of the reduction levels. For instance, the "Auto 1-5" means that the optimization process starts with reduction level 1. If the design does not fit the device after the completion of level 1, then it proceeds to level 2. If the design still does not fit the device, it proceeds to level 3 and so on until a fit occurs. Once the design achieves a device fit, the reduction level will be displayed in the Compile window (Figure 11-36).
 - There are five reduction levels, ranging from no logic reduction to group reduction with deMorganization of

outputs. The higher the level the better the utilization but the optimization time will also be longer. When compiling a design for the first time, it is recommended to use the "Auto 1-5" option. Note the level needed (displayed in the Compile window) to successfully compile the design. For subsequent compilations, select the single reduction level.

- **"Utilization"**: This command sets the maximum number of product terms (as a percentage) to be used during the logic optimization-process. For instance in the PA7024 device, if the product utilization is set as "Utilization = 60 %", then 60% of 80 product terms (80 product terms is the maximum for the PA7024) will be used during logic optimization. Hence, this command allows you to estimate whether additional logic can be implemented in the selected device. **The default product term utilization is "Utilization = 100 %"**.

Optimization Function

Level

Level 1	No reduction. Transforms equations to sum-of-products.
Level 2	Simple reduction. Combines duplicate product terms.
Level 3	Pin reduction. Optimizes terms per individual equation.
Level 4	Group reduction. Optimizes terms over all equations which can be shared.
Level 5	Group with output polarity inversion reduction. deMorganizes Outputs (automatically inverts polarity) to achieve best optimization of terms.
Auto 1-2	Optimizes from Level 1 to 2 until logic fits.
Auto 1-3	Optimizes from Level 1 to 3 until logic fits.
Auto 1-4	Optimizes from Level 1 to 4 until logic fits.
Auto 1-5	Optimizes from Level 1 to 5 until logic fits.
Utilization	Sets the maximum product terms which can be used in the logic reduction or optimization process. The number is set in percentage terms.

Table 11-3. "Settings" menu in the Compile menu window

Status	Displays the device utilization and use of architecture after the design is compiled.
Create .MAP file	During the fuse-mapping process, a ".MAP" file can be created in addition to the JEDEC file. This MAP file contains the detailed information regarding how each equation is mapped in the JEDEC file. The default condition is ON.

11.16 Simulate Operation - Waveform Screen

After successful compilation of a PSF design file, test-vectors can be used to verify the design. In the Simulate operation, these test-vectors are displayed as waveform signals (Figure 11-39). The vectors are created using the "Edit" command. The vectors are then used to simulate (logically only) the function of the design by retrieving the design's logic from the JEDEC file which was created during the compilation process. These vectors can also be appended to the JEDEC file so that they can be used to exercise the device after programming.

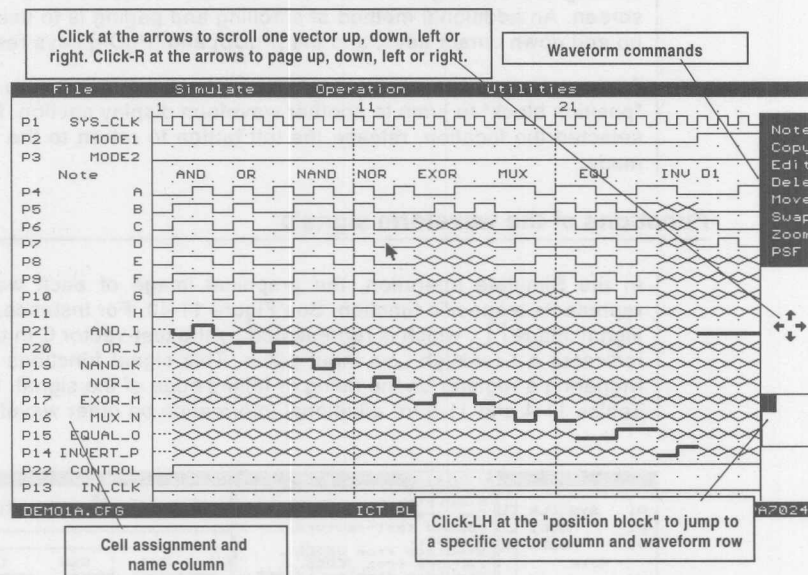


Figure 11-39. Simulate waveform screen



In the waveform display, each waveform row represents a signal from a pin or an internal node (e.g., a LCC, IOC or INC). The external pins are indicated by "P" followed by the pin number. LCC internal output is indicated by "L" with the cell assignment coordinates. The prefix for the IOC or INC node (i.e. the output of the IOC or INC register) is an "I" followed by the assigned pin number. The IOC and INC nodes are differentiated by the assigned pin numbers. For instance in the PA7140 PLCC device, pins 3-5, 19-21, 25-27 and 41-43 are assigned to INCs. The rest of the pins except pins 2 and 24 (CLK pins) are assigned to IOCs. For more information, please refer to the ICT data book.

Some examples of the waveform pin and cell assignments and labels are found in the TC7140.PSF example design file for the PLCC-packaged PA7140 (the PA7140 device has all the cells, i.e., LCCs, IOC's and INC's). These examples include:


P2	CLK	=> pin 2 with label CLK
L3A	P2	=> LCC 3A with label P2
I15	C2	=> IOC 15 with label C2
I4	SELECT	=> INC 4 with label SELECT

Scrolling and paging in the waveform display

As illustrated in Figure 11-39, scrolling and paging can be accomplished by clicking and clicking-R at the arrow markers located on the right side of the screen. An additional method of scrolling and paging is to use the left, right, up and down cursor keys, and the [PgUp] and [PgDn] keys respectively.

Alternately, you can click-LH (click and hold the left mouse button) at the "position block" to jump to another waveform display section. Once you have selected the location, release the left button to return to the normal screen mode.

Functions of the waveform signals

In the Simulate operation, the graphical image of each waveform signal represents a specific function. See Figure 11-40. For instance, the waveform signal image , which is represented by the test-vector C in the JEDEC file, indicates a Low-High-Low input pulse. This signal functions as a clock for triggering a register on the rising or falling edge of the signal. Please refer to Tables 11-4 and 11-5 for additional information on other waveform signals.

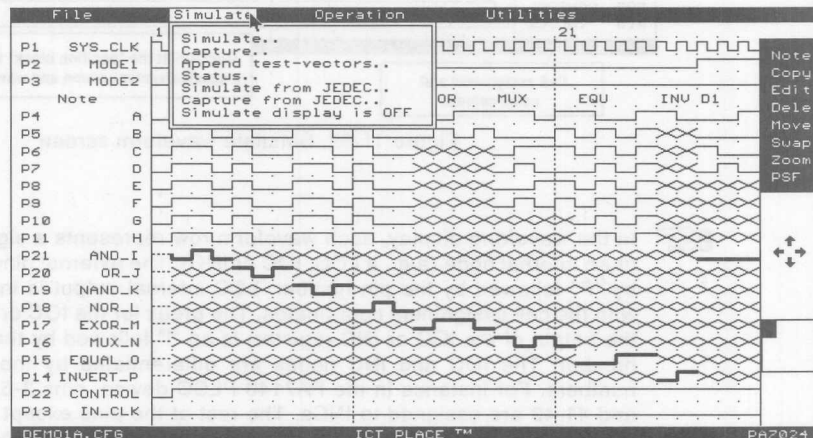


Figure 11-40. Simulate waveform screen










Symbol	Color	Function	JEDEC Vector Symbol
	Blue	System Clock	C
	Blue	Input High	1
	Blue	Input Low	0
	Blue	High Voltage Preload	P
	Blue	Input or Output Don't Care	X
	Yellow	Output High	H
	Yellow	Output Low	L
	Yellow	Output High Impedance	Z
	Red	Buried or Internal Signals which cannot be modified	N/A

Table 11-4. Waveform signal symbol table for a color monitor











Symbol	Linewidth	Function	JEDEC Vector Symbol
	Normal	System Clock	C
	Normal	Input High	1
	Normal	Input Low	0
	Normal	High Voltage Preload	P
	Normal	Input or Output Don't Care	X
	Thick	Output High	H
	Thick	Output Low	L
	Dotted	Output High Impedance	Z
	Center	Buried or Internal Signals which cannot be modified	N/A

Table 11-5. Waveform signal symbol table for a monochrome monitor

 Figures 11-39 through 11-54 illustrated in this section were captured via a monochrome monitor. Refer to Table 11-5 for the functions of the waveform signals in these figures.

11.17 Simulate Operation - Simulate Menu

Simulate Performs logic simulation of waveform vectors on external signals, i.e., on the "P" waveform rows only. The simulator compares the simulated signals with the current signals on the pins, and then marks the locations with signals that do not match. These marked locations are vector simulation errors (Figure 11-41). The special symbols used indicate the type of simulation errors (Table 11-6). On the other hand, the signals for all internal nodes are not checked but are automatically captured during logic simulation.

During simulation, the design's logic is retrieved from the JEDEC file that has the same root name. For example, the JEDEC file DEMO1A.JED will be used during the vector simulation of DEMO1A.CFG.

Capture Unlike the "Simulate" command, this command "captures" the signal on all external outputs. With this command, signals on the output pins need not be generated because the simulated signals are automatically inserted by the simulator. In addition, the simulated signals are also inserted into vector locations which contain the output Low "L", output High "H" and Don't Care "X" signals. This means that if you have simulation errors on any of these vector locations, they will be replaced by the simulated signals. See Figure 11-41.

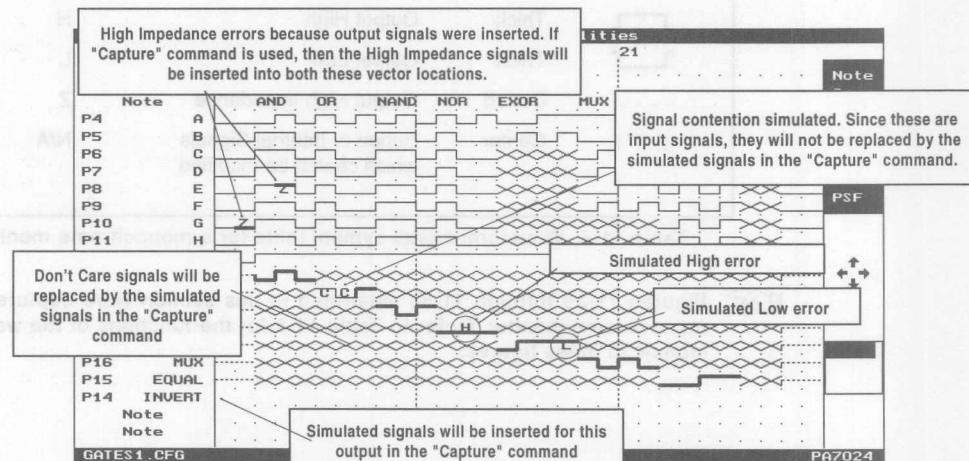


Figure 11-41. Vector simulate errors

Error Symbol	Function
L	Indicates that a LOW signal is simulated on the pin at the current vector location.
H	Indicates that a HIGH signal is simulated on the pin at the current vector location.
Z	Indicates that the pin is in a High Impedance condition at the current vector location. An example is the insertion of output signals ("L" or "H") on inputs.
C	Indicates that a signal contention condition exists at the current vector location. An example is the insertion of input signals ("0" or "1") on outputs.
U	Indicates that the signal at the current vector location is unstable or in an indeterminate state. An example of an application which causes this error is an oscillator. When an unstable error occurs, the simulation process is aborted and the pin number(s) reported.

Note that the PLACE Simulator will not flag an error if the unstable output has a Don't Care symbol.

Table 11-6. Simulation error symbols for pins



Please refer to Figure 11-42 for information on the "Simulate" and "Capture" commands for asynchronous clock designs.

Append test

vectors..... This command converts the waveform vectors into the JEDEC file test-vectors and appends them to the ".JED" file. This allows the vectors to exercise the device on a PLD programmer.

Status Provides status information such as the maximum vector columns available with the current system configuration (more system RAM memory, more vector columns available), number of total vectors used, number of simulation errors, and the previous simulation time.

Simulate from

JEDEC..... With this function, the PLACE Simulate waveforms can be generated from the test vectors specified in the JEDEC file. If an ICT PDS-3 programmer is present, this function together with the "Capture" function in the "Test" menu of the Program operation allows viewing of device vector results via the waveform screen.

Capture from

JEDEC..... This command is similar to that of the "Simulate from JEDEC" command except that the output signal levels will be replaced by the simulated signal levels.

Test Vectors for Asynchronous Clock Applications

Asynchronous clock refers to the triggering of the LCC or IOC register via a sum or product term. Devices with the asynchronous clock capability include PA7024, PA7128 and PA7140. If the simulated waveform vectors are appended to the JEDEC file for exercising the device, then special attention for the asynchronous clock designs is needed. This is because of possible data set-up time violations due to how the input signals are applied on the PLD programmer.



Note: On some programmers, the input signals are applied serially starting from pin 1 after the device has been powered-up (Vcc pin set to 5V). First, input signals "0" and "1" are applied, then preset signals "P" (this is a high voltage preset which is not supported in many PEEL devices), then clock signals ("C"), and then the output pins are sensed and compared with the vectors from the JEDEC file. With this method, data set-up time violations for asynchronous clock designs are very possible, especially if the input signals "0" and "1" are used to emulate the clock signals.

There are two methods to ensure proper test vectors for testing asynchronous clock designs.

1. The first method is to use the dedicated clock signal [] (JEDEC "C") in the sum or product term equation. Since this signal exhibits a Low-High-Low voltage level in a given vector period, the standard logic operation of the AND and OR operators may be applied, but with some modifications.

Clock	Operator	Input	Result
C	& (AND)	1	C
C	&	0	0
C	# (OR)	1	C
C	#	0	C

By using the dedicated clock signal, the programmer applies the signal to the clock only after all input signals are applied. Note that if the result "C" is routed to an external output, then a signal contention error will be flagged.

2. The second method is to add dummy or Wait states prior to all clock edges which are generated by the "0" and "1" input signals. The advantage with this method is that the same clock signal can be routed to an external output without encountering a signal contention simulation error as in the preceding method. However, the disadvantage is that a minimum of two vectors are required to generate a clock cycle, "0" and "1" signals on successive vectors.

Figure 11-42. Test Vectors for asynchronous clock applications - Sum or Product term clock

Preloading the LCC registers (in logic simulation only)

In the Simulate operation for the PA7024, PA7128 and PA7140 devices, all the LCC registers can be preloaded with user-specified data. Note that this feature is available only in software and does not exist in the device physically. If the preload vectors are applied to the device on a PLD programmer, these vectors will fail.

In Figure 11-44, the PA7024 application example has two sets of registered output pins P0..P7. At the preload vector column 11 and 22, the LCC registers for these outputs are preloaded with data 0 and FF HEX respectively. The preload condition is activated by the waveform symbol \ (JEDEC "P") on the dedicated preload pin 13 (each device type has a specific pin dedicated for the preload function). The clock symbol □ on pin 1 is not necessary because the preload symbol automatically loads the data asynchronously.

Below is a list of the preload pins and the assigned pins for the LCC registers for the PA7024, PA7128 and PA7140 devices.

Device	Preload Pin	Preload Data Pins	LCC Registers
PA7024 (DIP)	13	2 - 6	LCC 1A - 5A
		7 - 11	LCC 1B - 5B
		14 - 18	LCC 1C - 5C
		19 - 23	LCC 1D - 5D
PA7128	1	15 - 17	LCC 1A - 3A
		18 - 20	LCC 1B - 3B
		21 - 23	LCC 1C - 3C
		24 - 27	LCC 1D - 3D
PA7140 (PLCC)	24	6 - 11	LCC 1A - 6A
		12 - 16, 18	LCC 1B - 6B
		28 - 33	LCC 1C - 6C
		34 - 38, 40	LCC 1D - 6D

By adding the preload condition at the beginning of each CFG file (except for the first one), then up to 36 CFG files (CFA, CFB, ..., CFZ and CF0, CF1, ..., CF9) can be linked together for simulating a large PEEL Array design. With approximately 700 vectors per CFG file for a 512K system, about 25,000 "continuous" vectors can be simulated for a design.

Note: Preload feature is not available for JK registers.

11

Figure 11-43. LCC Register Preload function

Simulate

display When the Simulate display is set ON, the waveform vectors are displayed during the simulation or capture process. If this command is set OFF, the waveform vectors will not be displayed during simulation. Instead, each vector will be illustrated by a "." for a vector which passes simulation, and a "" for a failed vector.

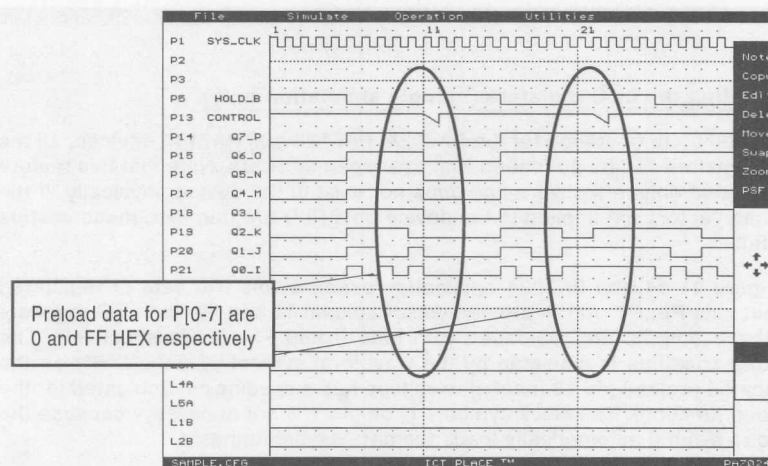


Figure 11-44. PA7024 LCC Register Preload, and Product or Sum Clock application

11.18 Simulation Operation - Entering or Editing Waveforms

In the Simulate operation, the test vectors are entered or modified via the "Edit" command. All other commands on the right side of the screen (such as Note, Copy, and etc.) are merely used for organizing the waveform screen. This means that these commands do not affect the results of the vector simulation. Please refer to Section 11.19 for more information on the waveform organization commands.

Note that only waveform signals for the external pins (inputs or outputs) can be entered or edited. All internal node signals are captured by the simulator and displayed for analysis.

Edit Edits input or output vectors, or inserts text into the rows generated by the Note command. There are three methods of entering or editing the waveform vectors.

1. Move the edit "box" cursor to a vector location and click the mouse button. Continue clicking until the desired waveform signal is displayed. Since there are eight different signals possible, each vector type is selected again after every eight clicks.
2. Move the edit cursor to a vector location and press the vector symbol keys such as C, 1, 0, P, H, L, X or Z to select the type of waveform signal. For instance, pressing the key "C" will select the clock signal for the current vector location. Refer to

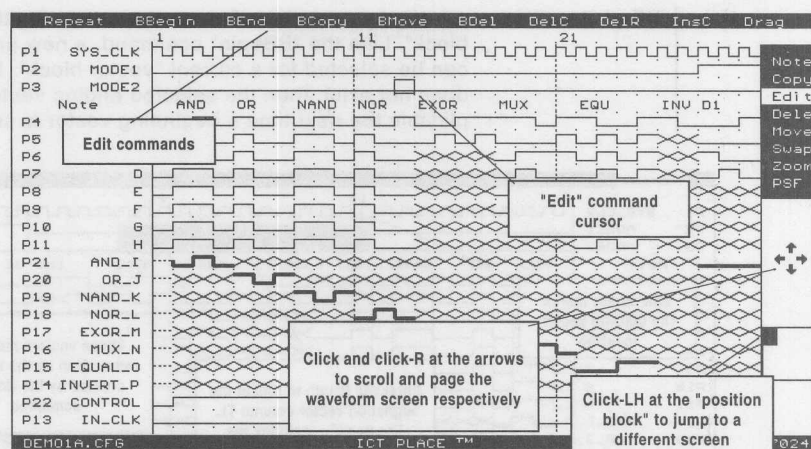


Figure 11-45. "Edit" command in the Simulate operation

Table 11-4 or 11-5 for the description of each waveform signal. Note that the vector symbols are actually the standard symbols used in the test vector section of the JEDEC file.

3. Use the "Drag" command which will be described later in this section.

Once the "Edit" command is selected, the advanced commands for editing test vectors will appear at the top of the screen and can be selected with the mouse. See Figure 11-45. In addition, the previous block of vectors selected via the BBegin and BEnd commands will be displayed. **Click-R to exit the "Edit" command.**

Repeat Repeat allows a single vector to be repeated by a specified number. Click "Repeat" then move the edit cursor to a vector location and click. This vector location will be the starting location. Then, enter the number of vectors to repeat and press Enter. All existing vectors following the starting vector will be overwritten. See Figure 11-46.

The commands which begin with the letter "B" indicate that they are block commands. Block commands are commands which manipulate a block of test vectors referred to as a "vector block" (Figure 11-47).

BBegin This command allows a vector location to be selected as the beginning vector of the "vector block". If no current block exists, then the PLACE software automatically enters the "BEnd" command immediately after the selection of the beginning vector. If a block exists, then a new beginning vector can be selected. The previous ending vector will remain unchanged.

BEnd Allows the selection of an ending vector for the "vector block". Like the "BBegin" command, a new ending vector can be selected for a current "vector block". If a block does not exist, then the selected ending vector is still applicable the next time a beginning vector is selected.

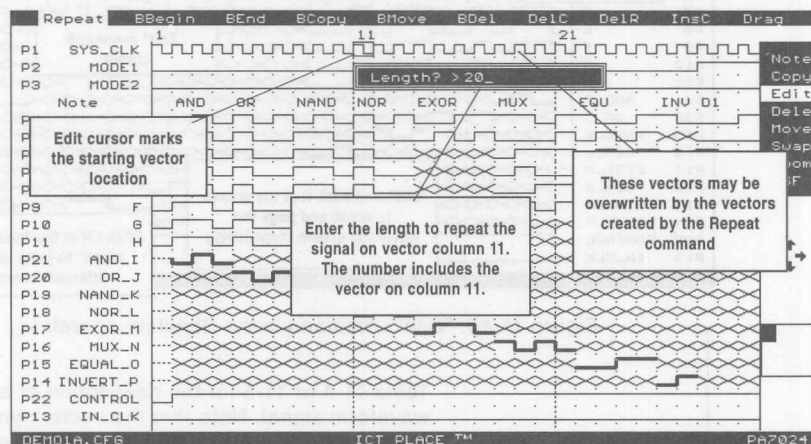


Figure 11-46. "Repeat" command



The beginning and ending vectors of the "vector block" must always be located on the upper-left and lower-right of the block respectively. A block can have a single row or column. In this case, the beginning vectors are the most-left or top vectors, and the ending vectors are the most-right or bottom vectors. In addition, beginning and ending vectors can be located on separate waveform screens.

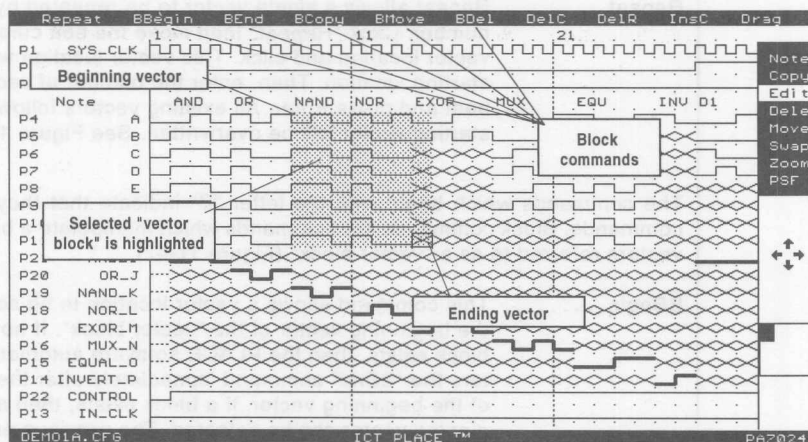


Figure 11-47. Vector block selected

- BCopy Copies the currently selected block into another waveform area after the selection of a starting vector location.
- BMove Moves the currently selected block into another waveform area after the selection of a starting vector location.
- BDel Deletes the currently selected block of vectors. A pop-up window to confirm the deletion will appear.

The following lists the row or column commands.

- DelC Enters a mode which allows the current waveform vector column to be deleted. Additional clicks will continue to delete the next vector column. Click-R to exit this mode.
- DelR Enters a mode which allows all the vectors on the selected waveform vector row to be deleted. Click-R to exit.
- InsC Enters a mode to allow vector columns to be inserted. The vector column is inserted prior to the selected vector column (Figure 11-48). Additionally, the signals on the new column follow the selected vector column.
- Drag Enters a mode which allows input or output signals to be entered or edited. Only four signals are available in the drag mode: input "0"; input "1"; output "L"; and output "H".

Select the waveform vector row and column after you have entered the "Drag" command. The drag edits will start from this location. Move the cursor horizontally across from left to right and click at the selected vector location to end the current signal. Click again to select

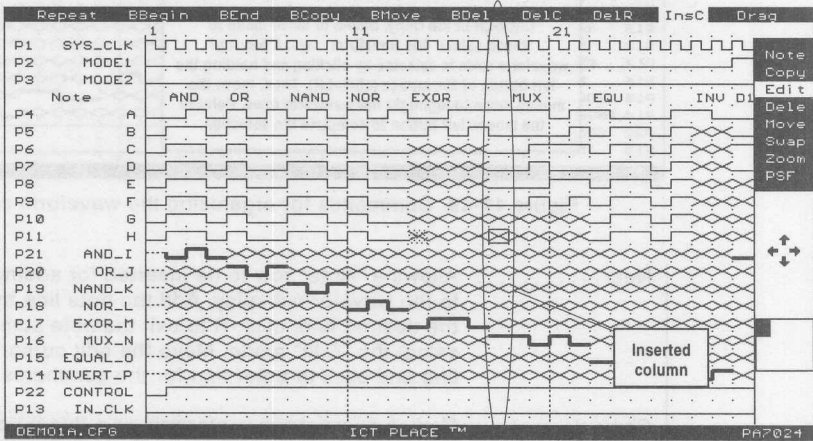


Figure 11-48. Inserting a vector column

another vector location. To exit the drag mode, click-R or press the [Esc] key. **Note that the drag edits will overwrite the previous vectors.**

Selecting the input or output signal

The input signal (blue or normal width) is selected when the "Drag" command is first selected. To "drag" an output signal, press ^X or [Ctrl]-X during the "dragging" process, i.e., the input signal is currently being dragged. Pressing [Ctrl]-X during the drag process toggles between dragging an input or an output signal. The output signal is indicated by a yellow or thick line.

11.19 Simulation Operation - Organizing Waveforms

All the commands in this section are used to organize the display of the waveform screen for a better understanding of PLACE designs. Therefore these commands do not affect the results of the simulation or the actual generation of the test-vectors for the JEDEC file. See Figure 11-49. In each CFG simulation file, a maximum of 99 waveform rows are allowed.

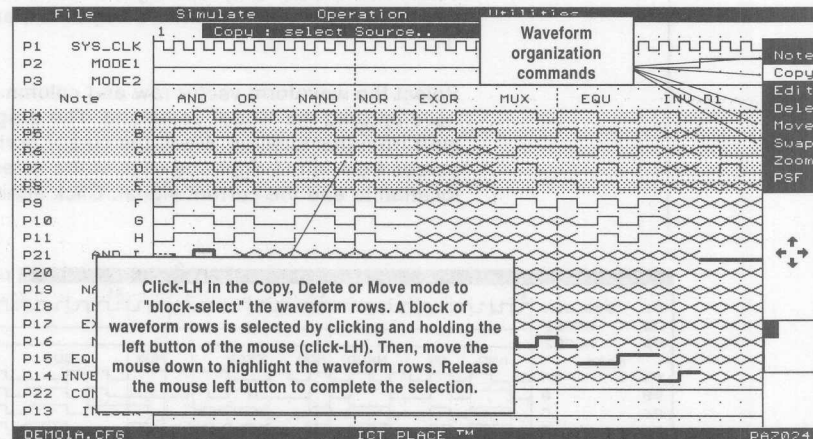


Figure 11-49. Commands for organizing the waveform screen

Note..... Allows a "Note" row to be inserted for adding comments to the waveform display. Add the note line by clicking at the desired line, click-R to exit the note command then select the "Edit" mode. Move the edit cursor to the note line and click to enter text for the comments.

Copy Copies a waveform vector row or a "block" of selected waveform rows to another location. This command will

prompt for a source and target selection. Click-R to exit this mode.

Dele Removes a waveform vector row or a "block" of selected waveform rows from the current waveform screen. Note that the unduplicated waveform rows for external pins and internal nodes will be appended to the bottom of the CFG file (last screen of the waveform display). All other waveform rows such as Notes and duplicated rows (i.e. rows that were copied using the "Copy" command) can be removed from the CFG file. The CFG file has a minimum number of waveform rows allocated for each device type that cannot be removed. For instance, the PA7024 device has 62 waveform signals (22 inputs/outputs + 20 LCC internal outputs + 20 IOC registered nodes) that are always present in the CFG file. Click-R to exit.

Move Allows a waveform vector row or a "block" of selected waveform rows to be moved from one location to another location. This command will prompt for a source and target selection. Click-R to exit.

Swap Allows a waveform vector row to be swapped with another vector row. This command will prompt for a source and target selection. Click-R to exit. No "block" swapping is available.

11.20 Simulate Operation - Zoom Command

When the **"Zoom"** command is selected, the waveform screen displays 170% more vectors than the normal screen. Normally, the waveform screen is 22 rows by 30 columns. But in the zoom mode, the screen is 30 rows by 60 columns. With more vectors being displayed, more waveform vectors can be viewed on a single screen, which may lead to a better understanding of the overall design.

Within the Zoom mode, there are actually two separate modes which will be referred to as Zoom Modes A and B. A typical procedure for using the Zoom mode is:

- From the normal waveform screen mode, click at the **"Zoom"** menu on the right side of the screen to enter Zoom Mode A. The screen in this mode consists of 30 rows of waveforms and 60 columns of vectors.
- In Mode A, almost all commands in the Simulate operation can be executed. These commands include file read and save, simulate, capture, or the PSF command (section 11.21). Some of the commands not executable in Mode A are the Note, Edit, Erase, Copy, Move and Swap commands. See Figure 11-50. If you click-R in Mode A, you will be returned to the normal waveform screen mode.
- To enter Mode B, click at the **"Zoom"** menu once again but this time don't release the left button of the mouse. A rectangular box depicting a window view of the current selected waveform screen is displayed (Figure 11-51).

This rectangular "view" window can be moved to another location by moving the mouse. If you wish to return to Mode A at this time, press the right button of the mouse while the left button is being pressed. Otherwise, releasing the left button of the mouse will return you to the normal waveform screen selected via the rectangular "view" window.

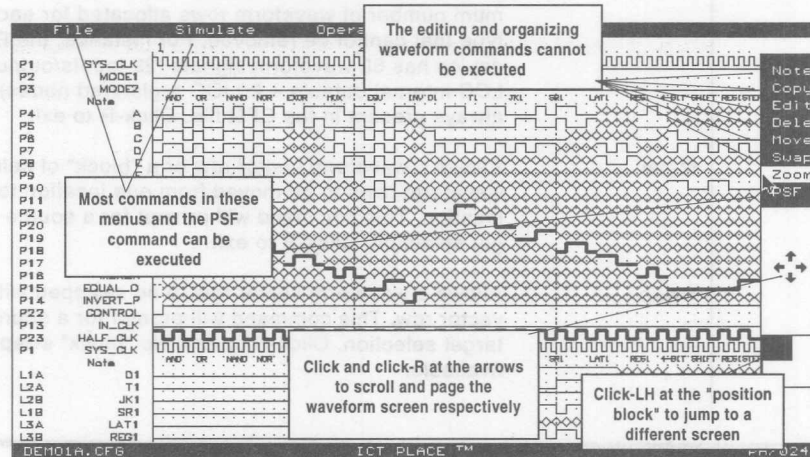


Figure 11-50. Mode A of the "Zoom" waveform screen

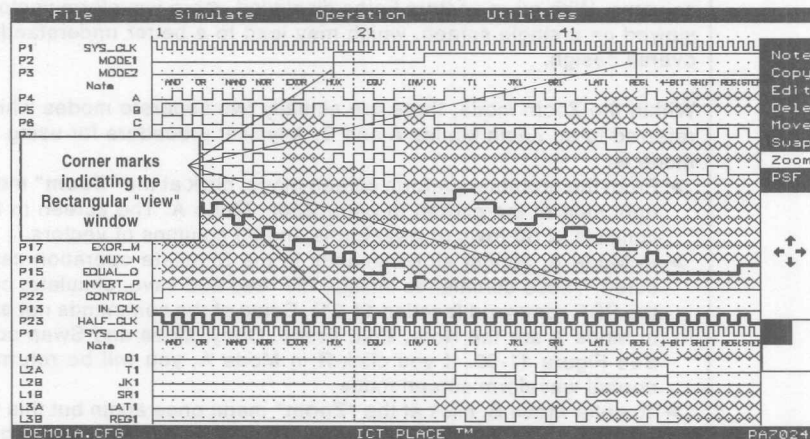


Figure 11-51. Mode B of the "Zoom" waveform screen

11.21 Simulate Operation - PSF Command

The PSF design file can be displayed on the waveform screen by selecting the "**PSF**" command located on the right side of the screen. See Figure 11-52. With the PLACE design source file displayed, you can compare the simulation results with the design logic. If a simulation waveform vector error is detected, then the modification can be done using the "Edit" command. If the error is in the design logic, then return to the Design operation to correct the error and recompile the PSF file.

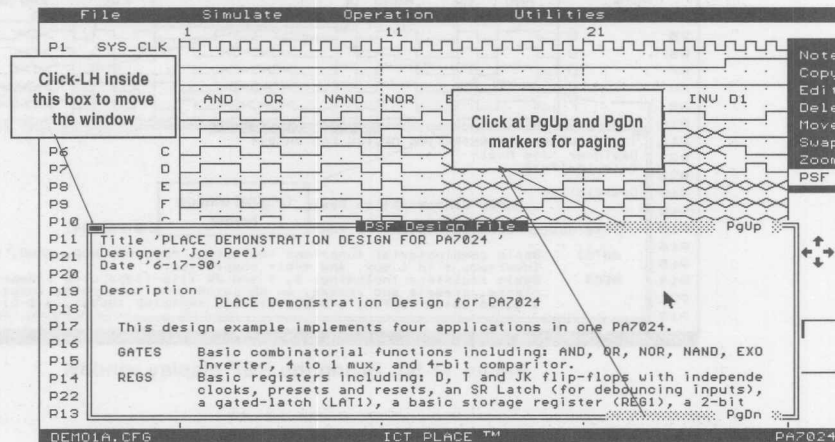


Figure 11-52. Displaying the PSF file on the waveform screen.

As shown in Figure 11-52, a window will pop-up displaying the PLACE design source file. The features of this window are similar to those available for the PSF Text Display windows found in the Design operation. These features include paging the display screen up and down and window sizing. An additional feature not available in the Design operation is moving the display window to another location (Figure 11-54). **To close the PSF window, press the [Esc] key or click-R.**

Paging Up and Down

As in the Design operation, paging can be done within the PSF window by clicking at the PgUp or PgDn markers located at the top and bottom of the window, or by pressing the PgUp and PgDn keys.

Sizing the Display Window

The size of the window can be adjusted by pressing the Up and Down cursor keys followed by the ENTER key. The Up cursor key increases the window size while the Down cursor key decreases the size. A maximum of 19 lines of text can be displayed in the window. See Figure 11-53.

Moving the Display Window

The window can be moved by clicking the left mouse button on the box in the upper left hand corner. Drag the window to the desired location, then release the mouse button. See Figure 11-54.

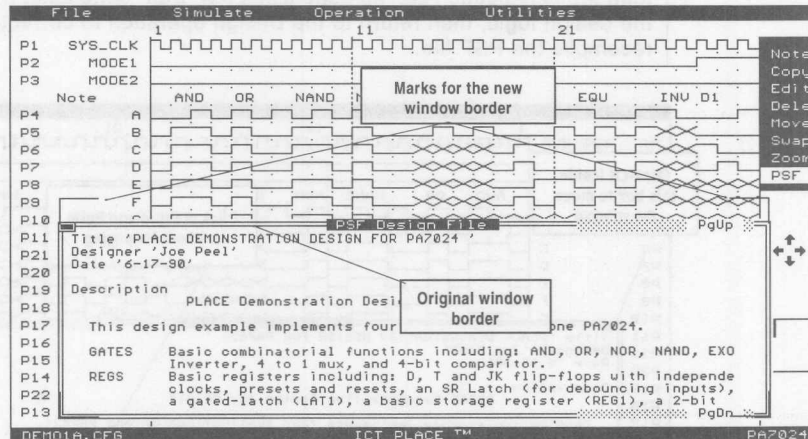


Figure 11-53. Sizing the PSF display window

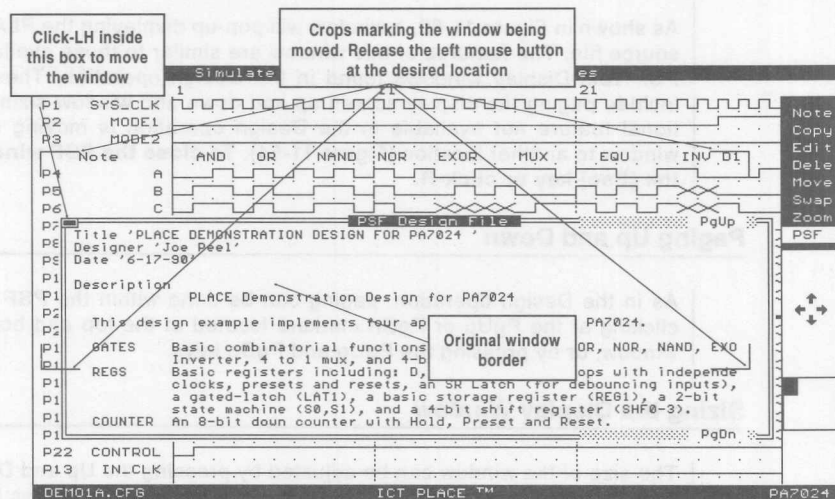


Figure 11-54. Moving the PSF display window.

11.22 Document Operation - Document Window

In the Document operation, the documents relating to a PLACE design can be printed via some of the most popular printers, such as IBM and Epson graphic printers, HP Laserjet II and postscript laser printers. In addition, the printing of these documents (including the design configuration and simulate waveform screen images, PSF design file, compiled outputs and etc.) can be set up in a queue or batch mode. Most printing options are self-explanatory; contact ICT if you need more information.

11.23 Document Operation - Waveform "Select" Print Option

The waveform "Select" option allows specific waveform screens to be selected for printing. A waveform screen can be selected by pressing the [SPACEBAR] key or clicking at the page number located at the upper-right corner of the screen. Once selected, the page number of the screen will be highlighted. For a list of selected waveform screens, click at the "List" command.

11.24 Document Operation - LCC/IOC or IOC "Select" Option

In PEEL Arrays, the LCC and IOC "Select" screen allows specific LCC/IOC pairs to be selected for printing. The selection is made by clicking at the LCCs or IOCs and the LCC/IOC pairs will be highlighted. In PEEL devices, the IOCs are selected with the similar method, i.e., clicking at the IOCs until highlighted.

11.25 Program Operation

If using a PDS series programmer (PDS-1, PDS-2, PDS-3) refer to the PDS user's Manual for information on program operation.

11.26 Program Operation - Serial Communication Window

The "PC Com" Interface window is automatically displayed if the ICT PDS series programmer is not installed in your computer. The commands in this window allow the JEDEC file to be transmitted or received via the COM port to or from a third-party programmer which has a serial communication file transfer utility.

11.27 PLACE Text Editor

The PLACE text editor (a Wordstar™-like editor) is used in the Design, Compile and Document operations. In the Design operation, the text editor is primarily used for entering or modifying the logic descriptions of the design. In the Compile operation, the editor is interfaced closely with the PLACE compiler. If a compilation syntax error is encountered, the editor opens automatically and displays the line with the error. If possible, this error can then be analyzed and modified without returning to the Design operation. In the Document operation, the editor is mainly used for displaying the JEDEC file.

Using a mouse in the editor

The PLACE text editor supports some of the editor commands via the mouse. Press and hold the middle or right button of the mouse (the button depends on whether a 2 or 3-button mouse is used) to enter the mouse mode. Once in the mouse mode, no text editing can be done. Instead, only screen paging and scrolling, and cursor movement can be performed. To exit the mouse mode, release the left button of the mouse. The best application of the mouse is to quickly move the editor cursor to another location.

Text Editor Keyboard Commands

Screen and cursor movement

Functions	Commands
Character left	^S or Left arrow key
Character right	^D or Right arrow key
Word left	^A or ^Left-arrow key
Word right	^F or ^Right arrow key
Line up	^E or Up arrow key
Line down	^X or Down arrow key
Scroll up	^W or ^Up-arrow key
Scroll down	^Z or ^Down-arrow key
Page up	^R or [PgUp] key
Page down	^C or [PgDn] key
Top of file	^QR or ^[PgUp] key
End of file	^QC or ^[PgDn] key
Begin of line	^QS or [Home] key
End of line	^QD or [End] key
Top of screen	^QE or ^[Home] key
Bottom of screen	^QX or ^[End] key
Top of block	^QB
Bottom of block	^QK
Previous cursor	^QP
Jump marker 0..3	^Q0..^Q3
Set marker 0..3	^K0..^K3

Insert and delete

Functions	Commands
New line	^M or [Enter] key
Insert line	^N
Tab	^I or [Tab] key
Delete current character	^G or [Del] key
Delete character left	^H or [Backspace] key
Delete word	^T
Delete to end of line	^QY
Delete line	^Y

Block Functions

In the Design operation, the PLACE software selects and highlights a block of text automatically when the editor is opened via the PSF Text Display windows. If desired, specific text can be manually "blocked" via the [F7] and [F8] function keys. This is done by first moving the editor cursor to the location which marks the beginning of the block and then press the [F7] key. Then, move the cursor to the "end" location of the block and press the [F8] key. A block is selected if it is highlighted.

Functions	Commands
Begin block	^KB or [F7] key
End Block	^KK or [F8] key
Copy block	^KC
Move block	^KV
Delete block	^KY
Hide block	^KH
Mark single word	^KT
Read block from file	^KR
Write block to file	^KW
Print block	^KP

Miscellaneous

Functions	Commands
Exit editor	^KQ or [Esc] key
Save and Open new file	^KD
Toggle insert mode	^V or [Ins] key
Toggle autoindent	^OI
Toggle fixed tabs/smart tabs	^OF
Restore line	^QL
Search string	^QF
Search and replace string	^QA
Repeat last search operation	^L

Insert and Delete

Functions	Commands
Delete line	DEL
Delete word	WD
Delete entire line	DEL
Delete character left	DEL
Delete word	WD
Delete to end of line	DEL
Delete line	DEL

Block Functions

In the Design operation, the PLACE software selects and highlights a block of text automatically when the editor is opened via the PSE Text Display window. If desired, specific text can be manually "blocked" via the [F7] and [F8] function keys. This is done by first placing the editor cursor in the location which marks the beginning of the block and then press the [F7] key. Then, move the cursor to the end location of the block and press the [F8] key. A block is created if it is highlighted.

Functions	Commands
Block block	BB or [F7] key
End block	EB or [F8] key
Copy block	CB
Move block	MB
Delete block	DB
Hide block	HB
Block single word	BS
Block block from file	BBF
Write block to file	WBF
Print block	PB

Miscellaneous

Functions	Commands
Exit editor	EO or [Esc] key
Save and Open new file	SO
Toggle insert mode	IM or [Ins] key
Toggle automatic	AO
Toggle line replacement mode	LR
Find line	FL
Search string	SR
Search and replace string	SCA
Repeat last search operation	LR

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PLACE Design Language

PLACE Design Language

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12.0 PLACE Design Language

12.1 Introduction

To simplify the design entry process, the PLACE software allows control of the architectures graphically. This capability allows the designer to better utilize his or her time on the actual design implementation and not on architectural syntax as in most other PLD software tools. Underneath the graphics however, the PLACE software incorporates a powerful design language that provides standard behavioral design methods such as State Diagrams, Truth Tables and Equations.

PLACE Source File Format

Figure 12-1 shows the format of the PLACE Source File (PSF). Figures 12-2 and 12-3 illustrate the differences between the PSF formats for the PA7024 and PEEL18CV8 devices. **Note: All format categories in Figure 12-1 that are shaded are automatically set-up via the PLACE architectural editor.**

Design Description:	<i>Title of the design, name of designer, date and detailed description of the design.</i>
Device type:	<i>PA7024, PEEL18CV8, PEEL22CV10A, etc.</i>
Special features:	<i>Sets Security-bit, Zero-Power or Signature Word.</i>
Input or Clock Pins:	<i>Assigns names to the clock and dedicated input pins.</i>
Cell Configurations:	<i>PEEL Arrays: IOC and LCC Configurations. PEEL Devices: IOC (Macro Cell) Configurations.</i>
Global Configurations:	<i>PEEL Arrays: Group A and B Global Cell Configurations. PEEL Devices: Asynchronous and Synchronous node definitions for registered PEEL Devices (e.g., PEEL18CV8, PEEL22CV10A, etc.).</i>
Comments	<i>Details the description of the design.</i>
Macro Definitions:	<i>State assignment, equation and constant declarations.</i>
State-diagrams	
Truth-tables	
Equations	

Figure 12-1. PLACE Source File Format



While reading the PSF file, the PLACE software checks the file format for incompatibilities. If any format incompatibilities are found for the selected device type, the PLACE software will display error messages.

```

TITLE ''
Designer ''
Date ''

Description
    Enter description here ...
End_Desc;

PA7024                                "Device type

"Optional Special Features Identifiers
AUTO_SECURE                          "Programs the security bit. If unspecified,
                                     "defaults to Security-bit OFF
SIGNATURE 'ABCDEFGH'                 "Programs Signature Word 'ABCDEFGH'

CLK1 PIN 1                           "Input or Clock pin declaration
CLK2 PIN 13

IOC ( 2 "POS IO ) <- 1A               "IOC Declaration
IOC ( 3 " POS IO ) <- 2A
IOC ( 4 " POS IO ) <- 3A
IOC ( 5 " POS IO ) <- 4A
IOC ( 6 " POS IO ) <- 5A
IOC ( 7 " POS IO ) <- 1B
IOC ( 8 " POS IO ) <- 2B
IOC ( 9 " POS IO ) <- 3B
IOC (10 " POS IO ) <- 4B
IOC (11 " POS IO ) <- 5B
IOC (14 " POS IO ) <- 1C
IOC (15 " POS IO ) <- 2C
IOC (16 " POS IO ) <- 3C
IOC (17 " POS IO ) <- 4C
IOC (18 " POS IO ) <- 5C
IOC (19 " POS IO ) <- 1D
IOC (20 " POS IO ) <- 2D
IOC (21 " POS IO ) <- 3D
IOC (22 " POS IO ) <- 4D
IOC (23 " POS IO ) <- 5D

```

Figure 12-2. PA7024 "ANew7024.PSF" File Template

LCC (1A " D POS REG REG)	"LCC Declaration
LCC (2A " D POS REG REG)	
LCC (3A " D POS REG REG)	
LCC (4A " D POS REG REG)	
LCC (5A " D POS REG REG)	
LCC (1B " D POS REG REG)	
LCC (2B " D POS REG REG)	
LCC (3B " D POS REG REG)	
LCC (4B " D POS REG REG)	
LCC (5B " D POS REG REG)	
LCC (1C " D POS REG REG)	
LCC (2C " D POS REG REG)	
LCC (3C " D POS REG REG)	
LCC (4C " D POS REG REG)	
LCC (5C " D POS REG REG)	
LCC (1D " D POS REG REG)	
LCC (2D " D POS REG REG)	
LCC (3D " D POS REG REG)	
LCC (4D " D POS REG REG)	
LCC (5D " D POS REG REG)	
Global = 1	"Number of global cells used
GBC (A Clk1 Clk1)	"Global Cell A configuration
GBC (B Clk1 Clk1)	"Global Cell B configuration
DEFINE	"Macro Definitions
STATE_DIAGRAM SD_name	"State diagram design syntax
END;	"Ends current State diagram syntax
TRUTH TABLE TT_name	"Truth table design syntax
END;	"Ends current State diagram syntax
EQUATIONS	"Logic equation syntax
"Equations for the Global Cell A	
RTA = 0;	"Reg-Type Product Term
PCLKA = 0;	"IOC Clock Product Term
PRESETA = 0;	"Preset Sum Term
RESETA = 0;	"Reset Sum Term
"Equations for the Global Cell B	
RTB = 0;	"Reg-Type Product Term
PCLKB = 0;	"IOC Clock Product Term
PRESETB = 0;	"Preset Sum Term
RESETB = 0;	"Reset Sum Term

Figure 12-2. PA7024 "ANEW7024.PSF" File Template (Continued)

```

TITLE ''
DESIGNER ''
DATE ''

Description
    Enter description here ...
End_Desc;

PEEL18CV8                                "Device type

"Optional Special Features Identifiers
AUTO_SECURE                             "Programs Security-bit. If unspecified,
                                         " defaults to security-bit OFF

CLK pin 1                               "Input or Clock pin declaration

IOC (12 " POS COM FEED_PIN )             "I/O or Macro Cell Configuration
IOC (13 " POS COM FEED_PIN )
IOC (14 " POS COM FEED_PIN )
IOC (15 " POS COM FEED_PIN )
IOC (16 " POS COM FEED_PIN )
IOC (17 " POS COM FEED_PIN )
IOC (18 " POS COM FEED_PIN )
IOC (19 " POS COM FEED_PIN )

AR NODE 21                              "Global Asynchronous Reset Node
SP NODE 22                              "Global Synchronous Preset Node

DEFINE                                  "Macro Definitions

STATE_DIAGRAM SD_name                   "State diagram design syntax
END;                                    "Ends current State diagram syntax

TRUTH TABLE TT_name                    "Truth table design syntax
END;                                    "Ends current State diagram syntax

EQUATIONS                               "Logic equation syntax

"Equations for the global nodes
AR = 0;                                "Global Asynchronous Reset Equation
SP = 0;                                "Global Synchronous Preset Equation

```

Figure 12-3. PEEL18CV8 "ANEWV8.PSF" Template File

12.2 Design Description

The design description section of the PSF format is made up of four fields. The fields include: Title of the design, Designer's name, Date of the design, and a detailed description of the design.



In describing the PSF formats for the following sections (including this one), *italics* will be used to identify fields in which the user would enter identifiers, such as title and date of the design, name of the designer, pin names, etc. The reserved identifiers will be specified in **bold**. Most of the examples used for illustrating the formats (except for the PEEL device formats) are taken from the Blackjack Machine Application Example (JACK7024.PSF) illustrated in section 13.7. **All reserved identifiers and labels are not case sensitive.**

Title

Format: Title '*title of design*'

Example: Title 'Blackjack Machine Example'

Only the characters between ASCII 32 and 127 can be used in specifying the title of the design. The maximum length of the title is 69 characters.



The characters between ASCII 32 and 127 are normal characters. These characters include A..Z, a..z, 0..9, space, !, ", \$, %, &, ', (,), *, +, ,, -, ., /, :, ;, <, =, >, ?, @, [, \,], ^, _, ` {, |, }, and ~.

Designer

Format: Designer '*name of the designer*'

Example: Designer 'Joe Peel'

Like the Title identifier, only characters between ASCII 32 and 127 can be used. The maximum length of the designer's string is 47 characters.

Date

Format: Date '*date of design*'

Example: Date 'May 10th, 1991'

Characters valid in the date string are between ASCII 32 and 127. The maximum string length is 47 characters.

Description

The Description identifier allows the user to specify in detail the description of the design. The user specifies his or her description within the reserved identifiers "**Description**" and "**End_Desc**". These identifiers are automatically inserted by the PLACE software.

Format: **Description**
 enter description of design here ...
 End_Desc;

Example: **Description**
 Blackjack Machine Example

This design example was based on C.R. Clare's design in Designing Logic Systems Using State Machines (McGraw Hill, 1972). The blackjack machine plays

All ASCII characters can be used here.

End_Desc;

All PLACE reserved words except "End_Desc" can be used within the "Description" and "End_Desc" identifiers. Each line does not need to begin with a double quotation mark, as required in the Comments field (Section 12.9).

12.3 Device Type

The target device of the design is declared by simply entering the ICT PEEL device name.

Format: *device_type*

The following are the device types supported in Version 2.71 or later of the PLACE software.

PA7024	PEEL22CV10A	PEEL18CV8	PEEL20CG10A
PA7128	PEEL22CV10A+	PEEL22CV8	PEEL22CV10AZ+
PA7140			

12.4 Special Features

Special features such as enabling the Security Bit, programming the Signature Word, and setting the Zero Power Bit are available for some of the PEEL devices. These features are optional, meaning that they are not required to be specified in the PSF file. If not specified, the default conditions will be implemented. Refer to the description of each of these features for their default conditions.

Security Bit

Once the security bit feature is enabled, the programmed data in the device (except for the Signature Word) is prevented from being loaded or read, and hence prevents any unauthorized copying of the design in the PEEL device.

The security bit feature is available for the following devices.

PA7024	PEEL18CV8	PEEL22CV8
PA7128	PEEL22CV10A+	PEEL20CG10A
PA7140	PEEL22CV10A	PEEL22CV10AZ+

Format: **AUTO_SECURE**

The security bit of the device is enabled via the reserved identifier **AUTO_SECURE**. If this identifier is specified in the PSF file, the PLACE Compiler will create a JEDEC file with the security bit enabled (sets the "G1" field). In most PLD programmers, the "G1" field automatically enables security bit programming.

Default condition: The **AUTO_SECURE** identifier is unspecified. The JEDEC file generated will not have the "G1" field. In most PLD programmers, the user can enable or disable security bit programming.

Signature Word

The signature word of the device allows a user to enter a design revision number so that the design can be identified after the security bit of the PEEL device is enabled. Hence, the signature word data can still be loaded even after the security bit of the device is enabled.

The signature word feature is supported in the following devices. Note that the number of 8-bit bytes in the signature word is specified within the parenthesis.

PA7024 (8 bytes)	PEEL22CV10A+ (3 bytes)
PA7128 (1 byte)	PEEL22CV10AZ+ (8 bytes)
PA7140 (2 bytes)	

Format: **SIGNATURE** 'signature str'

Example: Signature 'REV. A'

Default condition: **SIGNATURE** identifier is unspecified, which means that the signature word in the device JEDEC file is unused. Note that if the ICT PDS-1 programmer is present, this signature word can be programmed in the Program operation.

12.5 Clock and Input Pins

After labeling a clock or a dedicated input pin (a pin that is not associated with an Input Cell or INC) of the device using the **"Label"** command in the Design operation, the PLACE software automatically creates the pin assignment statement.

Format: *pin_label* **PIN** pin_number

Example: CLK1 pin 13

Please refer to Section 12.6 for the pin label format.

Default condition: An unlabeled pin (no pin assignment statement) signifies that the pin is unused.

12.6 Pin and Cell Labels

Format: First character: **A..Z, a..z, ~, /, !**
Body of the label: **A..Z, a..z, 0..9, ~, _**

Examples: Valid labels: Addr10, ~10, /OUT
Invalid labels: _Add, 25MHz, /15IN

The label is not case sensitive. The maximum length of the label is 8 characters (including the / or ! character). **When a / or ! character is added at the beginning of the label, the pin, cell or node becomes an active Low signal path.** Hence, a TRUE logic (logic "1") results when a Low signal is applied.

Example:
/A pin 1 "Active Low Input
B pin 2 "Active High Input

IOC (12 'C' Pos COM Feed_pin)	"Output Polarity = Pos
IOC (13 'D' Neg COM Feed_pin)	"Output Polarity = Neg
IOC (14 'E' Pos COM Feed_pin)	"Output Polarity = Pos
IOC (15 'F' Neg COM Feed_pin)	"Output Polarity = Neg

EQUATIONS
C.COM = A; "C=TRUE or 1 when A=LOW
D.COM = B; "D=TRUE or 1 when B=HIGH

The / or ! on the pin or cell labels only affect the active level of the inputs or feedback paths (i.e. variables on the right side of the equal sign in the equations). The polarity of the outputs (i.e. outputs routed to the external pins) is not affected because they are controlled by the IOC configuration statements. In the above example, the feedback active levels and output polarities of cells C, D, E, and F are:

Cell	Feedback Active Level	Output Polarity
C	High	High
D	High	Low
/E	Low	High
/F	Low	Low

12.7 Cell Configurations

The cell configuration format statements are used to specify the type of configuration of each cell in the selected device. In most cases, knowledge of the cell configuration formats is not necessary because the configurations of the IOC and LCC are automatically modified by the PLACE architectural software.



Note that all the configuration statements are necessary for the operation of the PLACE software. This means that **you should not delete any of these configuration statements** including the configuration statements for unused cells.

Format:

Input Cell in PA7128 and PA7140:

INC (pin_number 'pin_label' input_type)

Example: INC (3 'A1' Reg)

I/O Cell in PEEL Arrays:

IOC (pin_number 'pin_label' output_pol pin_type) <- Assigned_LCC

Example: IOC (4 'V4' Pos IO) <- 3A

Logic Control Cell in PEEL Arrays only:

LCC (cell_number 'cell_label' flip-flop_type clock buried_out ext_out)

Example: LCC (1A 'ADD10' D SumC Reg Reg)

I/O Cell (or Macro Cell) in PEEL devices:

IOC (pin_number 'pin_label' output_pol pin_type feedback_type)

Example: IOC (12 'OUT' POS COM FEED_PIN)

Default condition: The default cell configurations are set by the cell configuration statements in the "ANEWxxxx.PSF" files. If the **"New"** function under the File menu command in the Design operation is selected, the PLACE software reads the ANEW file for the selected device (see Table 12-1) and sets the default configurations found in the file.

ANEW File	Device
ANEW7024.PSF	PA7024
ANEW7140.PSF	PA7140
ANEW7128.PSF	PA7128
ANEWV8.PSF	PEEL18CV8
ANEW2CV8.PSF	PEEL22CV8
ANEWG10A.PSF	PEEL20CG10A
ANEWV10A.PSF	PEEL22CV10A
ANEWV10P.PSF	PEEL22CV10A+
ANEWVAZP.PSF	PEEL22CV10AZ+

Table 12-1. PLACE ANEW Template Files

Parameters for the INC Format (PA7128 and PA7140 only)

Pin_Number	The pin number that is assigned to the current Input cell.	
Pin_Label	Device	INC Pin Numbers
	PA7128	2-6, 8-14
	PA7140 (PLCC)	3-5, 19-21, 25-27, 41-43
	PA7140 (DIP)	2-4, 17-19, 22-24, 37-39
Input_type	The identifiers for the pin type parameter are:	
	Identifier	Function
	COM	Combinatorial input
	REG	D-type registered input
	LAT	D-type latched input

Parameters for the IOC Format (PEEL Arrays only)

Pin_Number	The pin number that is assigned to the current I/O cell.	
Pin_Label	Device	IOC Pin Numbers
	PA7024	2-11, 14-23
	PA7128	15-20, 22-27
	PA7140 (PLCC)	6-16, 18, 28-38, 40
	PA7140 (DIP)	5-16, 25-36
See Section 12.6 for the format of the pin label.		

Output_pol	<p>This parameter which refers to the output polarity of the pin is controlled by the following identifiers:</p> <table><tr><th>Identifier</th><th>Function</th></tr><tr><td>POS</td><td>Positive Polarity for the Output</td></tr><tr><td>NEG</td><td>Negative Polarity for the Output</td></tr></table> <p>The output polarity "bubble" in the Design operation of the PLACE software controls this parameter. Inserting the / or ! character in the pin_label does not affect the output (Section 12.6).</p>	Identifier	Function	POS	Positive Polarity for the Output	NEG	Negative Polarity for the Output																				
Identifier	Function																										
POS	Positive Polarity for the Output																										
NEG	Negative Polarity for the Output																										
Pin_type	<p>The identifiers for the pin type parameter are:</p> <table><tr><th>Identifier</th><th>Function</th></tr><tr><td>IO</td><td>I/O</td></tr><tr><td>REG</td><td>I/O with D-type registered input</td></tr><tr><td>LAT</td><td>I/O with D-type latched input</td></tr><tr><td>OUT</td><td>Output only</td></tr><tr><td>INCOM</td><td>Input only</td></tr><tr><td>INREG</td><td>Input only with D-type register</td></tr><tr><td>INLAT</td><td>Input only with D-type latch</td></tr><tr><td>OUTREG</td><td>Output only with D-type registered feedback</td></tr><tr><td>OUTLAT</td><td>Output only with D-type latched feedback</td></tr><tr><td>DCOM</td><td>Output only with feedback from Sum-D</td></tr><tr><td>DREG</td><td>Output only with D-type registered feedback from Sum-D</td></tr><tr><td>DLAT</td><td>Output only with D-type latched feedback from Sum-D</td></tr></table> <p>The parameters DCOM, DREG and DLAT are only applicable for PA7128 and PA7140 devices.</p>	Identifier	Function	IO	I/O	REG	I/O with D-type registered input	LAT	I/O with D-type latched input	OUT	Output only	INCOM	Input only	INREG	Input only with D-type register	INLAT	Input only with D-type latch	OUTREG	Output only with D-type registered feedback	OUTLAT	Output only with D-type latched feedback	DCOM	Output only with feedback from Sum-D	DREG	Output only with D-type registered feedback from Sum-D	DLAT	Output only with D-type latched feedback from Sum-D
Identifier	Function																										
IO	I/O																										
REG	I/O with D-type registered input																										
LAT	I/O with D-type latched input																										
OUT	Output only																										
INCOM	Input only																										
INREG	Input only with D-type register																										
INLAT	Input only with D-type latch																										
OUTREG	Output only with D-type registered feedback																										
OUTLAT	Output only with D-type latched feedback																										
DCOM	Output only with feedback from Sum-D																										
DREG	Output only with D-type registered feedback from Sum-D																										
DLAT	Output only with D-type latched feedback from Sum-D																										
Assigned_LCC	<p>The LCC that is connected to the current IOC.</p>																										

Parameters for the LCC Format (PEEL Arrays only)

Cell_number	<p>The cell number that is assigned to the current Logic Control cell. It ranges from 1A-6A, 1B-6B, 1C-6C and 1D-6D. Figure 12-4 illustrates the cell number organization for the PA7024 device.</p> <table><tr><th>Device</th><th>LCC Assignments</th></tr><tr><td>PA7024</td><td>1A-5A, 1B-5B, 1C-5C, 1D-5D</td></tr><tr><td>PA7128</td><td>1A-3A, 1B-3B, 1C-3C, 1D-3D</td></tr><tr><td>PA7140 (PLCC)</td><td>1A-6A, 1B-6B, 1C-6C, 1D-6D</td></tr></table> <p>Refer to the IOC statement described in the previous section for the assigned IOC for each LCC.</p>	Device	LCC Assignments	PA7024	1A-5A, 1B-5B, 1C-5C, 1D-5D	PA7128	1A-3A, 1B-3B, 1C-3C, 1D-3D	PA7140 (PLCC)	1A-6A, 1B-6B, 1C-6C, 1D-6D
Device	LCC Assignments								
PA7024	1A-5A, 1B-5B, 1C-5C, 1D-5D								
PA7128	1A-3A, 1B-3B, 1C-3C, 1D-3D								
PA7140 (PLCC)	1A-6A, 1B-6B, 1C-6C, 1D-6D								
Cell_label	<p>Refer to Section 12.6 for the cell label format.</p>								

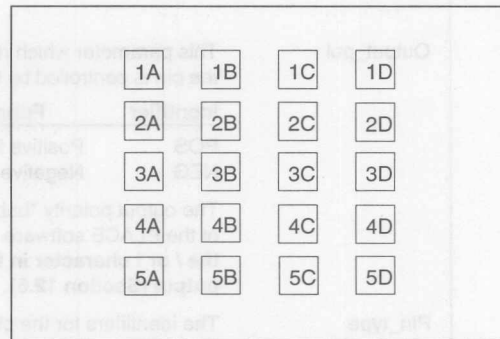


Figure 12-4. LCC numbering system in PA7024

Flip-flop type

Specifies the type of register in the LCC. The dynamic register type setting (RT signal) is also specified in this parameter. The RT signal which comes from the Global Cell dynamically changes the register type in the LCC during normal (5V) operation.

Identifier	Function
D	D-type register (RT mode is disabled)
T	T-type register (RT mode is disabled)
JK	JK-type register (RT mode is disabled)
DT	D-type register when RT= FALSE, T-type register when RT = TRUE
DJK	D-type register when RT = FALSE, JK-type register when RT = TRUE
TD	T-type register when RT = FALSE, D-type register when RT = TRUE
JKD	JK-type register when RT = FALSE, D-type register when RT = TRUE

Clock

Controls the type of clock for the current LCC.

Identifier	Function
POS	High speed (system) clock from an Input/Clock pin that triggers the register on the rising edge. Note: Global cell controls which pin to use for system clock.
NEG	Register is triggered on the falling edge of the system clock.
SumC	Local clock coming from the Sum C term. Register is triggered on the rising edge of the clock signal.
SumD	Local clock coming from the Sum D term. Register is triggered on the falling edge of the clock signal.

Buried_Out	Output of the LCC that is fed back internally to the array.										
<table> <tr> <th>Identifier</th><th>Function</th></tr> <tr> <td>Reg</td><td>Internal output from the register</td></tr> <tr> <td>SumA</td><td>Internal output from the Sum A term (i.e. the input of the register)</td></tr> <tr> <td>SumB</td><td>Internal output from the Sum B term</td></tr> <tr> <td>SumC</td><td>Internal output from the Sum C term</td></tr> </table>		Identifier	Function	Reg	Internal output from the register	SumA	Internal output from the Sum A term (i.e. the input of the register)	SumB	Internal output from the Sum B term	SumC	Internal output from the Sum C term
Identifier	Function										
Reg	Internal output from the register										
SumA	Internal output from the Sum A term (i.e. the input of the register)										
SumB	Internal output from the Sum B term										
SumC	Internal output from the Sum C term										
Ext_Out	Output of the LCC to the I/O cell. This output sends the signal from inside the device to the outside world. The final output signal depends on the output polarity of its assigned IOC.										

Parameters for the IOC Format (PEEL Devices)

Pin_Number	The pin number that is assigned to the current I/O cell.												
Pin_Label	See section 12.6 for the format of the I/O pin label.												
Output_pol	This parameter which refers to the output polarity of the pin is controlled by the following identifiers: <table> <tr> <th>Identifier</th><th>Function</th></tr> <tr> <td>POS</td><td>Positive Polarity for the Output</td></tr> <tr> <td>NEG</td><td>Negative Polarity for the Output</td></tr> </table> <p>The output polarity "bubble" in the PLACE architectural software controls this parameter. Inserting the / or ! character in the pin_label does not affect the output (Section 12.6). Hence, only this parameter controls the polarity of the output.</p>	Identifier	Function	POS	Positive Polarity for the Output	NEG	Negative Polarity for the Output						
Identifier	Function												
POS	Positive Polarity for the Output												
NEG	Negative Polarity for the Output												
Pin_type	The identifiers for the pin type parameter are: <table> <tr> <th>Identifier</th><th>Function</th></tr> <tr> <td>COM</td><td>I/O with combinatorial output</td></tr> <tr> <td>REG</td><td>I/O with D-type registered output</td></tr> <tr> <td>OUTCOM</td><td>Combinatorial output only</td></tr> <tr> <td>OUTREG</td><td>Registered output only</td></tr> <tr> <td>IN</td><td>Output disabled (may or may not be an input depending on the feedback type)</td></tr> </table>	Identifier	Function	COM	I/O with combinatorial output	REG	I/O with D-type registered output	OUTCOM	Combinatorial output only	OUTREG	Registered output only	IN	Output disabled (may or may not be an input depending on the feedback type)
Identifier	Function												
COM	I/O with combinatorial output												
REG	I/O with D-type registered output												
OUTCOM	Combinatorial output only												
OUTREG	Registered output only												
IN	Output disabled (may or may not be an input depending on the feedback type)												
Feedback_type	Specifies the type of feedback for the selected device. This parameter is applicable for all PEEL Devices except the 16V8, 20V8, and 22CV10A which follow the industry-standard architectures. Note that the feedback selection is available on the 22CV10A+. The feedback types of the 22CV10A are automatically set to FEED_PIN and FEED_REG for COM and REG output types respectively. <table> <tr> <th>Identifier</th><th>Function</th></tr> <tr> <td>FEED_PIN</td><td>Feedback from the pin</td></tr> <tr> <td>FEED_REG</td><td>Feedback from the output of the register</td></tr> <tr> <td>FEED_OR</td><td>Feedback directly from sum term (i.e. prior to the register)</td></tr> </table>	Identifier	Function	FEED_PIN	Feedback from the pin	FEED_REG	Feedback from the output of the register	FEED_OR	Feedback directly from sum term (i.e. prior to the register)				
Identifier	Function												
FEED_PIN	Feedback from the pin												
FEED_REG	Feedback from the output of the register												
FEED_OR	Feedback directly from sum term (i.e. prior to the register)												

12.8 Global Configurations

PEEL Arrays

The global configurations for PEEL Arrays are used to set up the global signals for the LCCs, IOCs and INCs.

Format: Global = n "n = 1 or 2 cells
 GBC (A LCC_clock IOC_clock) "Global Cell A
 GBC (B LCC_clock IOC_clock) "Global Cell B
 GBC (C INC_clock) "Global Cell C
 "(PA7140 and
 "PA7128 only)

Example: Global = 1
 GBC (A Clk1 Clk2)
 GBC (B Clk1 Clk2)
 GBC (C Clk1)

Table 12-2 shows the definitions of the Clk1, Clk2 and PClk terms used in the GBC configuration statements.

Clk1 and Clk2 terms - specify the system clock pin to use.

Device	Clk1 pin	Clk2 pin
PA7024 (DIP, SOIC)	1	13
PA7024 (PLCC)	2	16
PA7128	1	28
PA7140 (PLCC)	2	24
PA7140 (DIP)	1	21

PClk terms - specify to use the product term for the global clock.

Device	IOCs by PClkA	IOCs by PClkB	INCs by PClkC
PA7024 (DIP, SOIC)	2 - 11	14 - 23	none
PA7024 (PLCC)	3-7, 9-13	17-21, 23-27	
PA7128	15 - 20, 22 - 27		2-6, 8-14
PA7140 (PLCC)	6 - 16, 18	28 - 38, 40	3-5, 19-21, 25-27, 41-44
PA7140 (DIP)	5-16	25-36	2-4, 17-19 22-24, 37-39

Table 12-2. Definitions of global clock terms

Global = n

The **n** parameter equals 1 or 2. This parameter sets the number of global cells to be used for the LCCs and IOCs. If one global cell is used, then global cell A controls the global signals for all LCCs and IOCs in the device and the global cell B configuration statement is ignored. If "Global = 2" is specified, then Global Cell A controls the global signals for the IOCs and LCCs in which the IOCs are on the left side of the device. Global Cell B then controls the global signals for the IOCs and LCCs in which the IOCs are on the right side of the device. See Table 12-2.

Below are the descriptions of each parameter in the GBC (GBC A, B or C) configuration statements.

LCC_clock

Sets the system clock pin for the LCC global clock. The two options available are the **Clk1** and **Clk2** pins. Refer to Table 12-2 for the Clk1 and Clk2 pin numbers for each PEEL Array.

IOC_clock

Sets the system clock pin or product term for the IOC global clock. The options available are **Clk1**, **Clk2**, **PCLKA** and **PCLKB**. See Table 12-2.

INC_clock

Sets the system clock pin or product term for the INC global clock. The options available are **Clk1**, **Clk2** and **PCLKC**. See Table 12-2.

PEEL Devices

In the registered PEEL devices such as the PEEL18CV8, 22CV10A, and 22CV10A+, the global configurations are represented by the global node assignments. These global nodes control the asynchronous reset and synchronous preset product terms.

Format: *node_label* **NODE** *node_number*

Example: AR node 21 Asynchronous reset for PEEL18CV8 device

node_label Please refer to section 12.6 for the node label format.

node_number The node assignment numbers for the selected device are:

Device	Node Number	Function
PEEL18CV8	21	Asynchronous Reset (AR)
	22	Synchronous Preset (SP)
PEEL22CV8	25	Asynchronous Reset (AR)
PEEL20CG10A	26	Synchronous Preset (SP)
PEEL22CV10A		
PEEL22CV10A+		
PEEL22CV10AZ+	25	Asynchronous Reset (AR)
	26	Synchronous Preset (SP)
	27	P-Term Clock (CS)

12.9 Comments

In the PLACE software, comments are available so that each component of the design which may not be readily apparent from the source file is explained. Comments do not affect the design itself. Liberal use of comments can make a PSF design file easy to understand.

Format: " Insert comments here ...

Example: "Enable security bit programming

A comment begins with a double quotation mark (") and ends with the end of line. A comment can be specified anywhere in the PSF design file.



Note that the double quotation marks are not required if the comments are specified within the **"DESCRIPTION"** and **"END_DESC"** reserved identifiers.

12.10 Macro Definitions

The macro definitions are used for:

- declaring constants which make the design easier to understand
- declaring commonly used equations so they don't have to be repeated throughout the design file
- assigning the state cells and set variables for state diagram designs
- assigning the pins or cells for truth table designs

The macro definitions in the PSF design file are located after the reserved identifier **DEFINE** but prior to one of the following reserved identifiers: **STATE_DIAGRAMS**; **TRUTH_TABLE**; or **EQUATIONS** (whichever is specified first). Macro definitions that are specified via the "Macro" function in the Design operation are automatically inserted into this location.

Format: **DEFINE**
specify macro definitions here...

STATE_DIAGRAMS, TRUTH_TABLE or EQUATIONS

Example:

DEFINE

QSTATE = [ADD10 SUB10 Q2 Q1 Q0]

Clear = ^B00000

ShowHit = ^B00001

AddCard = ^B11011

Add_10 = ^B10010

Wait = ^B00010

Test_17 = ^B00110

Test_22 = ^B00111

"State_Diagram Assignment

"Constant Declaration

ShowStand	=	^B00101	
ShowBust	=	^B00100	
is_Ace = !V4 & !V3 & !V2 & !V1 & V0;			"Equation Declaration
SCORE	=	[S4 S3 S2 S1 S0]	"Truth table input assignment
BCD2	=	[D5 D4]	"Truth table output assignment
BCD1	=	[D3 D2 D1 D0]	"Truth table output assignment
STATE_DIAGRAM QSTATE			"Ends the Macro Definitions

Macro Constants

Format: *Const_label = constant*

Examples: Clear = ^B00000
ShowHit = ^B00001

Const_label The format for the label of the constant is similar to that of the pin or cell label (see Section 12.6) with two exceptions, and they are:

1. The length of the label can be up to 20 characters long instead of 8.
2. The / or ! character cannot be used at the beginning of the label.

Constant Specifies the value of the constant in decimal, hexadecimal, octal or binary numbering system.

The format for the constant is:
symbol + number

The symbols for the numbering systems are:

Numbering system	Symbol
Decimal	none (default)
Hexadecimal	^H or ^h
Octal	^O or ^o
Binary	^B or ^b
Examples:	15 (decimal) ^HF (hexadecimal) ^O17 (octal) ^B1111 (binary)

Macro Equations

Format: *Eqn_label = complex_eqn*

Example: Is_ACS = !V4 & !V3 & !V2 & !V1 & !V0;

Eqn_label The label for the equation macro is similar to that for the label for the macro constant. See previous section.

Complex_eqn

Macro equation can be specified using the logic operators (), !, &, # and \$ (refer to Section 12.13).

The input side of a macro equation (i.e. the right side of the "=" symbol) is made up of pin or cell labels, or labels from other macro equations. Below is an example of a macro equation which is a function of other macro equations.

DEFINE

```
Mac1 = A & B;           "Macro level 1
Mac2 = C # D;           "Macro level 1
Mac3 = Mac1 $ Mac2;     "Macro level 2
```

If the macro equation uses only pin and/or cell labels, then it has one macro level. If it uses **previously defined** macro equation labels in addition to the pin and cell labels, then it has multiple macro levels. The number of macro levels depends on whether the macro equation labels used in the equation are functions of more macro equation labels themselves.

The number of macro levels is limited by the total number of characters (**maximum of 1024 characters**) in the "flattened" macro equation, i.e. the input side of a flattened macro equation consists of only pin and/or cell labels. Note that the additional spaces between the input variables in the macro equation are automatically deleted by the PLACE Compiler. Example: A maximum of 5 macro levels can be used if each (unflattened) equation level has less than 200 characters. **Typically, the maximum macro level is about ten.**

Macro State Cell Assignments for STATE DIAGRAMS

The state cell assignment defines the pin or cell labels to be used by the state diagram design syntax.



The **"Allocate"** command in the "Design" menu window of the Design operation automatically generates the state cell assignment definition and STATE_DIAGRAM design syntax. An example is shown below.

DEFINE

```
QSTATE = [ADD10 SUB10 Q2 Q1 Q0]
```

```
STATE_DIAGRAM QSTATE
```

```
"enter design here ...
```

```
END;
```

Format: *state_label* = [Cell1 Cell2 Cell3 ... CellN]

Example: QSTATE = [ADD10 SUB10 Q2 Q1 Q0]

State_label

The state label format is similar to that of the pin or cell label (Section 12.6). The only exception is that the state

	label does not allow the use of the / or ! character at the beginning of the label.
Cell(n)	Specifies the cell labels to be used as state cells by the state diagram. A maximum of 24 cells can be allocated as state cells. Each state cell label must be separated by a space. The most and least significant bit of the state cells are the first and last allocated cells respectively in the cell assignment definition, i.e. Cell1 is the Most Significant Bit and Celln is the Least Significant Bit.

Macro Set Variables in State Diagrams

Outputs in a state diagram can be assigned to a set variable so that the logic of these outputs can be specified with a numeric constant. The constant can be specified in a binary, octal, hexadecimal or decimal (default) numbering system.

Format: `set_var = [Cell1 Cell2 Cell3 ... Celln]`

Example:

```

DEFINE
TEST = [T2 T1]           "State cell assignment
OUT = [Y3 Y2 Y1 Y0]      "Set variable assignment

STATE_DIAGRAM TEST
State 0:   OUT = 0;       "Macro Set variable OUT
              "Y3-0 = 0000
              Goto 1;
State 1:   OUT = ^HB;     "Y3-0 = 1011
              Goto 2;
State 2:   OUT = ^B1100;  "Y3-0 = 1100
              Goto 3;
State 3:   Goto 0
END;
```

Set_var The format is similar to the state label format used for the state cell assignments.

Celln Specifies the assigned pin or cell label.

The macro set variable equation feature is only available within the state diagram design syntax. Also, **only one macro level is available in the macro set variable assignment.**

Macro Cell Allocation for Truth Tables

The "**Allocate**" command in the PLACE Design operation can also be used to allocate the pins and cells for the truth table design. The pins and cells can be allocated as truth table inputs, truth table outputs or both. If a cell or pin is allocated as the truth table input and output, then it is an I/O. The output of the I/O is then enabled or disabled via the .OE equation.

The following example shows the allocation of the pins and cells for the truth table design "TABLE1".

Example: TRUTH_TABLE TABLE1
(I4 I3 I2 I1 I0 -> Y5 Y4 Y3 Y2 Y1 Y0)
END;

Another method of allocating the pins and cells is through the macro set variable method. The inputs and outputs of the truth table can be assigned to the macro set variables in the DEFINE section. The labels of these macro set variables are then used in the truth table design syntax instead of the pin and cell labels.

Format: *table_label* = [*Cell1 Cell2 Cell3 ... Celln*]

Example: DEFINE
Input = [I4 I3 I2 I1 I0];
Y_HiBit = [Y5 Y4];
Y_LoBit = [Y3 Y2 Y1 Y0];

TRUTH_TABLE TABLE1
(Input -> Y_HiBit Y_LoBit)
^H15 -> 1 ^HA "I4-0 = 10101, Y5-0 = 011010
^H16 -> 1 ^HB "I4-0 = 10110, Y5-0 = 011011
END;

Table_label The format is similar to the state label used for the state cell assignments.

Celln Specifies the assigned pin or cell label.

Please refer to Section 12.12 on "Truth Table Design Syntax" for more information.

Macro Counter Function

COUNTERF is the macro function for designing an up-down, loadable counter. It must be specified in the DEFINE section.

Format COUNTERF(*Load, Updown, cBits, Type, iBits*)

Example:

DEFINE

UPDN_BITS = [Q4 Q3 Q2 Q1 Q0]; "Counting Bits. Q[4-0] can be pin
"or cell labels.

LOAD_EN = A & B; "Load Control Equation. Loads
"when A = TRUE and B = TRUE.

LOAD_BITS = [L4 L3 L2 L1 L0]; "Load Inputs, either pin or cell
"labels

```
UPDN_CON = C & !D;
```

"Updown Control. If C=TRUE, D=FALSE, it is DOWN Counter else, it is Up Counter.

```
COUNTERF(Load_en, UPDN_CON, UPDN_BITS, T, Load_BITS);
```

EQUATIONS

Load: 0 = No load function

Pin_Name, Node_Name (Cell_Names),
Macro_defined_label = load control

Updown: 0 = Up Ccount

1 = Down Count

Pin_Name, Node_Name (Cell_Names),
Macro_defined_label = updown control

(True logic for Up Count)

cBits: A Macro-Set-Variable with at least 2 elements.

This set contains the counting bits which include

Pin_Names or Node_Names (Cell_Names).

Type: D = D-type counter

T = T-type counter (uses fewest # of product terms)

(The pins or cells assigned to the macro label in the "cBits" parameter must have the same register type.)

iBits: 0 = Non-loadable counter

Macro-Set_Variable = Data bits for loading the counter. This set must have the same number of elements as the cBits.

The elements include Pin_Names or Node_Names

(Cell_Names). If load=0, then iBits=0.

12.11 State Diagrams

The state diagram language is used to implement state machine designs. In the PLACE software, state machine designs are specified between the **"STATE_DIAGRAM *state_label*"** and **"END"** identifiers. These identifiers together with the state cell allocation definition (refer to Section 12.10) are automatically created when the LCCs or IOCs are allocated for the state machine via the **"Allocate"** command in the Design operation.

Format:

DEFINE

```
State_label = [Cell1 Cell2 ... Celln]
```

STATE_DIAGRAM *State_label*

```
STATE state_0: "usually Reset state"
```

STATE *state_1*:

•

•

```
STATE state_n: "last state"
```

END;

<i>State_label</i>	The state label format is similar to that of the pin or cell label (See section 12.6). The only exception is that the state label does not allow the use of the / or ! character at the beginning of the label.
<i>Celln</i>	Specifies the cell labels to be used as state cells by the state diagram. A maximum of 24 cells can be allocated as state cells. Each state cell label must be separated by a space. The most and least significant bit of the state cells are the first and last allocated cells respectively, i.e., Cell0 and Celln are MSB and LSB respectively.
<i>State_n</i>	Specifies the state number which can be in the form of a numeric value or a constant label defined in the DEFINE section. Refer to "Macro Constants" in Section 12.10.

The PLACE state diagram syntax includes:

- **GOTO**
- **IF-THEN-ELSE**
- **CASE-ELSE-ENDCASE**
- **WITH-ENDWITH;**
(used in conjunction with GOTO, IF-THEN-ELSE and CASE-ELSE-ENDCASE)

GOTO

Format: GOTO *state_num*;

Examples: GOTO ShowHit; or
GOTO ^B00001;

State_num Specifies the state number for the unconditional jump. A numeric representation of the state or a constant label defining the numeric value in the macro definition section can be used to indicate the state number.

The GOTO statement is used to unconditionally jump to a different state on the next clock edge.

IF-THEN-ELSE

Unlike the GOTO statement, the IF statement provides a conditional jump to the next state. If the condition is satisfied, the logic jumps to the state specified after the THEN identifier. If the condition is not satisfied, the ELSE state will be the next state.

Format: IF *condition* THEN *state_num1*
ELSE *state_num2*;

Example: if (!CARDIN) then AddCard
 else ShowHit; ^B00001 can be used
 "instead of ShowHit.

Condition A boolean expression condition which can be in the form of a macro equation label (see "Macro Equations" in Section 12.10).

State_num1 If condition is satisfied, then jump to this state on the next clock edge.

State_num2 If condition is not satisfied, then jump to the alternate state.

CASE-ELSE-ENDCASE

Format: **CASE**
 condition_1: state_num;
 condition_2: state_num;
 .
 .
 condition_N: state_num;
 "ELSE is optional
 state_num;
 ENDCASE;

Example: case
 !Bust: ShowStand;
 Bust & !Ace: ShowBust;
 Bust & Ace: Sub_10;
 endcase; ^B01111 can be used
 "instead of the constant label
 "Sub_10.

Condition_N The condition must be a boolean expression. It can also be in the form of an equation label defined in the macro definition section (see "Equation Declaration" in Macro Definitions).

State_num The number represents the state for the conditional jump.

The CASE statement is simply an IF statement with multiple conditions. It lists a sequence of mutually-exclusive conditions and their corresponding state numbers. If a condition in the list is satisfied, the logic jumps to the corresponding state on the next clock edge. If no conditions are satisfied, then it jumps to the state number specified after the ELSE reserved identifier.



Note that the ELSE identifier is optional. If it is not specified and the conditions in the CASE list are not satisfied, then the next state is dependent on the type of flip-flop that is set up in the state cells. For instance, if the state cells have D-type registers, then the next state will reset to state 0. If the state cells have T-type registers, then it will hold at the current state.

WITH-ENDWITH

The WITH statement is used in conjunction with the GOTO, CASE-ELSE-ENDCASE or IF-THEN-ELSE statements. It allows outputs to be specified so that they use the same clock edge (rising or falling clock edge dependent on the configuration) that triggers the next state. **ICT recommends using only registered outputs with the WITH statement.**

Format: WITH *registered output equations ...*
ENDWITH;

```
Example:   if (A & B) then 1 with
           C = IN; "C is a D-type registered output
           D = 1;  "D is a T-type registered output
           endwith;
           else 2;
```

In the above example, when the expression (A & B) is true jump to state 1 on the next clock edge. Using the same clock edge, the output C latches the data from the input IN. Also, output D will toggle (since it is a T-type register) on same clock edge. If the condition (A & B) is not satisfied, the logic jumps to state 2 without changing the signals on outputs C and D.

Register Types of the "allocated" state cells

Prior to entering your state diagram design syntax, the outputs of the allocated LCCs and IOCs must be configured as registered outputs. The type of registers used, whether they are D, T or JK type registers, affect the behavior of the state diagram. An example is shown in Figure 12-5.

Outputs of the State Diagram

The two types of outputs in the PLACE state diagram are the synchronous and asynchronous outputs.

- **Synchronous Outputs:** These are registered outputs which use the same clock as the state machine. The outputs follow the input data on the next clock edge.
- **Asynchronous Outputs:** These are combinatorial outputs. The outputs follow the input data immediately.



Note that the state diagram outputs must first be configured using the PLACE architectural software. For instance if a registered output is required, the type of flip-flop (D,T or JK) and clock (pin or sum term) must be configured in the LCC/IOC or IOC screen in the Design operation.

The two classes of state machine designs that can be created using the PLACE software are the Mealy and Moore machines. Both of these state machine designs can utilize synchronous and asynchronous outputs.

<pre> DEFINE ST_TEST = [S2 S1 S0] STATE_DIAGRAM ST_TEST state 0: goto 1; state 1: case A&B&C: 0; A&B&C: 3; /A&B&C: 4; end; state 2: goto 5; . state 7: goto 0; END: </pre>	
<p>All conditions in the case statement of state 1 failed. Hence, the equations for the state cells S0, S1 and S2 are:</p> $S0 = 0; S1 = 0; S2 = 0;$ <p>Question: What is the next state?</p>	
<p>If D-type registers are used for S0, S1 and S3 state cells:</p> <p>Answer: Outputs of D-type registers follow the input on the next clock edge. Hence after clocking the S0, S1 and S2 registers, the outputs equate to 0 which is the condition of state 0. So, state 0 is the next state.</p>	<p>If T-type registers are used for S0, S1 and S3 state cells:</p> <p>Answer: Outputs of T-type registers follow the previous state on the next clock edge if the inputs are FALSE or "0". Hence after clocking the S0, S1 and S2 registers, the outputs follow the previous state of each register. So, state 1 is next state.</p>

Figure 12-5. State diagrams with D and T type registers

Mealy Machine

A Mealy state machine is defined as having outputs which are a function of two sets of variables:

- the present input conditions
- the present state of the machine

Examples: Me_Reg = INPUT; "Registered output
 Me_Com = INPUT; "Combinatorial output

Moore machine

A Moore state machine is defined as having outputs which are strictly a function of the state of the machine.

Examples: Mo_Reg = 0; "Registered output
 Mo_Com = 0; "Combinatorial output

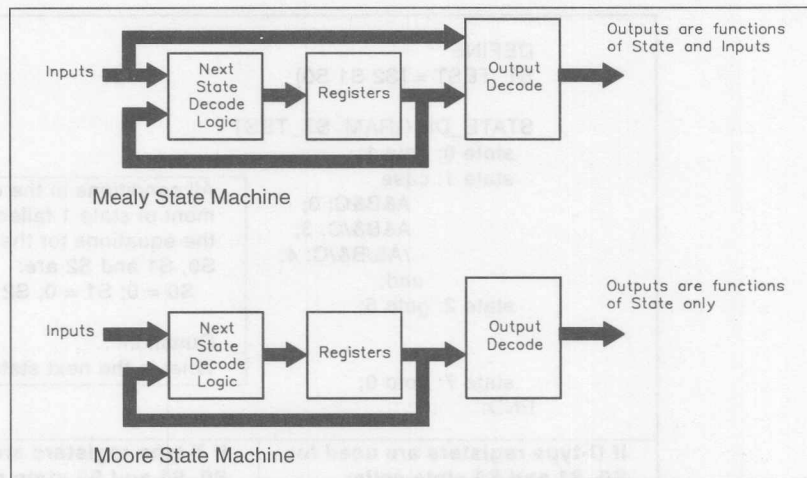


Figure 12-6. Mealy and Moore State Machines

How the PLACE State Diagram works

Figure 12-7 shows a state diagram example (SDEXAMPL.PSF) using the PLACE state diagram language. This example does not implement any specific application except to illustrate the usage of the state diagram language. The features that are illustrated in the example are:

- GOTO, CASE-ELSE-ENDCASE, IF-THEN-ELSE and WITH-END-WITH syntax.
- Synchronous and asynchronous outputs in Mealy and Moore state machines
- Set Equations for Moore Machine Applications (refer to Section 12.10 on "Macro Definitions")

12.12 Truth Tables

In addition to state diagrams and equations, truth tables can be used to describe the logic designs.

Format 1: TRUTH_TABLE *table_label*
(*In1 In2 ... InN -> Out1 Out2 ... OutN*)

END;

Format 2: TRUTH_TABLE *table_label*
(*Input -> Output*)

END;

DEFINE

EXAMPLE = [S1 S0]

"State cell assignment definition

Grp_Out = [OUT3 OUT2 OUT1 OUT0]

"Group outputs assignment

St0 = 0;

"default - Decimal

St1 = ^H1;

" ^H - Hexadecimal

St2 = ^O2;

" ^O - Octal

St3 = ^B11;

" ^B - Binary

In0 = /I2 & /I1 & /I0

"Input conditions for the State Diagram

In1 = /I2 & /I1 & I0

In2 = /I2 & I1 & /I0

In3 = /I2 & I1 & I0

In4 = I2 & /I1 & /I0

In5 = I2 & /I1 & I0

In6 = I2 & I1 & /I0

In7 = I2 & I1 & I0

In4T06 = In4 # In5 # In6

STATE_DIAGRAM EXAMPLE

"Goes to STATE St0 upon device power-up (all registers reset on power-up)

STATE St0:

Mo_Reg = 0;

"Moore registered output

Mo_Com = 0;

"Moore combinatorial output

Grp_Out = 0;

"Moore group combinatorial output, Out3-0 = 0000

Me_Reg = INPUT;

"Mealy register output

Me_Com = INPUT;

"Mealy combinatorial output

IF In1 THEN St1

"If In1=true, then go to STATE St1,

ELSE St0

" else remain at STATE St0.

STATE St1:

Grp_Out = ^B0110;

"Out3-0 = 0110. These combinatorial outputs will be valid after the
"present state occurs with a single propagation delay (tpd).

Me_Reg = INPUT;

"This registered output will be valid on the next clock edge,
" i.e. clock edge for the NEXT STATE (St0, St1 or St2 depending
"on which CASE condition is satisfied).

Figure 12-7. PLACE State Diagram Language for SDEXAMPL Design Example

```

Me_Com = INPUT; "This combinatorial output will be valid after the present
                 "state occurs with a single propagation delay (tpd).

CASE
  /I2 & I1 & /I0: St0      "Go to St0 if (/I2&I1&/I0)=In2=true
    WITH
      Mo_Reg = 1; "This output equals to 1 on the next clock edge
                  "only if the NEXT STATE is St0.
    ENDWITH;
  In3:      St2;      "Go to St2 if In3=true
ELSE
  St1      "If no condition in the CASE list is satisfied, remain at STATE St1.
ENDCASE;
STATE St2:
  Grp_Out = ^HA;      "Out3-0 = 1010. These combinatorial outputs will be valid after the
                      "present state occurs with a single propagation delay (tpd).

  IF (In4To6)      THEN St3      "If (In4To6)=true, then go to STATE St3
    WITH
      Me_Reg = INPUT;      "This registered output will be valid on the next
                          "clock edge only if the NEXT STATE is St3.
    ENDWITH;
  ELSE
    St2;      "If (In4To6)=false, then remain at STATE St2.

STATE St3:
  Mo_Reg = 1;      "This output equals 1 on the next clock edge.
  Mo_Com = 1;      "This combinatorial output will be valid after the present state
                  "occurs with a single propagation delay (tpd).
  Grp_Out = 0;      "Out3-0 = 0000.
  Me_Reg = 0;      "Reset all Mealy outputs
  Me_Com = 0;

  GOTO St0;      "Go to STATE St0 unconditionally.
END;      "End of STATE DIAGRAM EXAMPLE

```

Figure 12-7. PLACE State Diagram Language for SDEXAMPL Design Example (Continued)

Example 1: TRUTH_TABLE DECODE "3-to-8 Decoder
(C B A -> Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7)
0 0 0 -> 1 0 0 0 0 0 0 0
0 0 1 -> 0 1 0 0 0 0 0 0
0 1 0 -> 0 0 1 0 0 0 0 0

END;

Example 2: DEFINE
SCORE = [S4 S3 S2 S1 S0]
BCD2 = [D5 D4]
BCD1 = [D3 D2 D1 D0]

TRUTH_TABLE BIN2BCD "From JACK7024.PSF
(SCORE -> BCD2 BCD1)

0 -> 0 0;
1 -> 0 1;
2 -> 0 2;

END;

Table_label The format for the label is similar to that for the pin or cell label (Section 12.6) with one exception, and that is the / or ! character is not allowed at the beginning of the label.

InN (Format 1) Specifies the pin or cell labels to be used as truth table inputs. The inputs can be either registered or combinatorial. **Input data must be in binary (0 or 1) format.**

OutN (Format 1) Specifies the pin or cell labels to be used as truth table outputs. Like the inputs, truth table outputs can be either registered or combinatorial. **Output data must be in binary (0 or 1) format.**

Inputs (Format 2) Specifies a macro defined group of registered or combinatorial pins or cells to be used as truth table inputs. Input data can be in decimal (default), hexadecimal (^H or ^h), octal (^O or ^o) or binary (^B or ^b) numbering system. Only one macro level is available for the macro input set.

Outputs (Format 2) Specifies a macro define group of registered or combinatorial pins or cells to be used as truth table outputs. Input data can be in a decimal (default), hexadecimal (^H or ^h), octal (^O or ^o) or binary (^B or ^b) numbering system. Only one macro level is available for the macro output set.

An additional feature is that both the truth table formats can be used in a single truth table design.

Alternate truth table description which uses both formats for Example 2 is:

```

      TRUTH_TABLE BIN2BCD
      ( SCORE -> D5 D4 BCD1)
        0 -> 0 0 0;
        1 -> 0 0 1;
        2 -> 0 0 2;
        .
        .
      END;

```

12.13 Equations

The boolean logic equations are the primary methods for specifying logic functions in the PLACE software.

The PLACE architectural software automatically creates the equation for each sum or product term in the cell when it is labeled via the "**Label**" command in the "Design" menu of the Design operation. An example of a newly labeled LCC is shown below.

```

A.D = 0;
A.AP = 0;
A.AR = 0;
A.CLK = 0;

```

Format: *Output_label.EXT = logic_equation ;*

(The semicolon at the end of the equation is used by the PLACE software to mark the end of the equation when displaying the equation in the Equation Display window. Refer to "PSF Text Display Windows" in Section 12.12.)

Examples: C1.COM = (V0 & Add10 & Sub10 & S0);
 S0.T = (V0 & Add10 & Sub10);
 XOR1.COM = A \$ B;
 XOR2.COM = (!A & B) + (A & !B);

Output_label This is the pin or cell label that has been entered via the "**Label**" command. Refer to Section 12.6 for the format of the label.

.EXT The dot extension of the output is automatically appended to the output label by the PLACE software. The type of extension that is appended on each output label depends on the configuration of the pin or cell, the specific function of the product or sum term, and the device type. Refer to Figure 12-8.

Logic_equation A boolean logic expression that consists of inputs, feedbacks and logic operators. Table 12-3 shows the functions and priorities of the logic operators available in the PLACE software.

Operator	Logic Function	Priority
()	Logical organization	1
! or /	NOT	2
& or *	AND	3
# or +	OR	4
\$	Exclusive-OR	5

Table 12-3. Priorities of logic operators in PLACE



The output equations can be moved to other locations of the PSF design file as long as they are specified after the reserved identifier **EQUATIONS**. However, the PLACE software operation will be affected if the unused or any other equations generated by the PLACE software are deleted. This means that all equations, whether they are used or unused, are continuously referenced by the PLACE software.

Functions of the Dot Extensions in the equation labels

In the PLACE source file, each of the Dot extensions represents a specific function. Figure 12-8 details the functions of all Dot extensions.

Logic Reduction Compiler Directive (For Equations Only)

A compiler directive is available to prevent redundant terms in the equations from being removed during the logic optimization process. Sometimes redundant terms are intentionally added to avoid race or hazard conditions, especially in asynchronous applications.

Format: @REDUCE ON or @R+

@REDUCE OFF or @R-

Example: @R- "same as @Reduce Off
 G_Latch.COM = "Gated Latch Application
 LAT_EN & LAT_IN
 !LAT_EN & G_Latch
 LAT_IN & G_Latch; "redundant term to fix hazard
 @R+ "same as @Reduce On

@Reduce On Equations following this directive will be optimized. Redundant terms will be removed from the equations. This is the default condition.

@Reduce Off All equations specified after this directive will be flattened (i.e. converted to Sum-of-Product equations from complex equations) but not optimized. Redundant terms will be left in the equations.

PEEL Arrays		
Sum Term	Dot Extension	LCC Function (unless stated otherwise)
Sum A	.COM	Combinatorial Internal/External Output
	.D	D Input of the Register
	.T	T Input of the Register
	.J	J Input of the Register
	.SumA	Sum A term is unused
Sum B	.COM	Combinatorial Internal/External Output
	.K	K Input of the Register
	.AP	Asynchronous Preset for Register
	.SumB	Sum B term is unused
Sum C	.COM	Combinatorial Internal/External Output
	.CLK	Asynchronous Clock for Register
	.AR	Asynchronous Reset for Register
	.SumC	Sum C term is unused
Sum D	.CLK	Asynchronous Clock for Register
	.OE	External Output Enable Control (IOC)
	.FB	Buried feedback (PA7128 and PA7140)
	.SumD	Sum D term is unused
PEEL Devices		
Prod Term	Dot Extension	Function
And A	.OE	External Output Enable Control
	.AndA or .And	Product (AND) term A is unused

Figure 12-8. Functions of the Dot Extension in the Equations Labels

Equations of the Outputs used for State Diagrams or Truth Tables

Boolean equations are generated for all pins and cells that are labeled via the "Label" command, including those that are specifically used for state diagram or truth table designs. **These equations if they are unmodified do not affect the logic of the state diagrams or truth tables because they always equate to zero.** However, if the equations are modified and they do not equate to zero, then they will be logically ORed with the boolean equations that are transformed from the state diagram or truth table design syntax by the PLACE compiler.

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Application Examples

13.0 PLACE Application Examples

13.1 Overview

There are several PLACE application examples provided with the PLACE software; these are listed in Table 13-1. The following pages provide descriptions and block diagrams for the most important of the design examples. The design source (PSF) files with equation, state machine, and truth table descriptions are not shown. Please use the PLACE software to review the design source files. The PLACE document operation can also be useful for printing out the PSF design files or other applicable graphics and text files.

File Name	Device	Description
*DEMO1A.PSF	PA7024	Demonstration design for the PA7024 which includes Basic Gates and Registers, 8-bit Down Counter, 2-bit State Machine, 4-bit Shift Register and 8-bit Bidirectional I/O Port
BI_PORT.PSF	PA7024	8-bit Bidirectional I/O Port (part of DEMO1A)
COUNTER1.PSF	PA7024	8-bit Down Counter with Preset, Reset and Hold (part of DEMO1A)
*TIMER.PSF	PA7024	16-Bit Programmable Clock Generator/Timer
*JACK7024.PSF	PA7024	Blackjack Machine Example
*TC7140.PSF	PA7140	8-bit Time/Counter
*ST7128.PSF	PA7128	4-bit State Machine and 8-bit Counter
*V8GATES.PSF	18CV8	Basic Logic Gates
*V8REGS.PSF	18CV8	Basic Registers and Latches
*V8CLKADD.PSF	18CV8	Clock Divider Address Decoder
V8BUSMUX.PSF	18CV8	Bus Programmable 8-to-1 Multiplexer
V8FCNTR.PSF	18CV8	8-bit Counter with Function Controls
V8CPORT.PSF	18CV8	Change-of-State Input Port with Interrupt
V8SYNC.PSF	18CV8	Synchronization Circuit.
V10CNT8.PSF	22CV10	8-bit Up/Down Loadable Counter with Carry-out or Borrow-in
PARV10A.PSF	22CV10A	9-bit Even/Odd Parity Generator/Checker
V10ZPORT.PSF	22CV10A+	Change-of-State Input Port with Interrupt
ONE_HOT.PSF	22CV10A+	One-Hot State Machine

* Design descriptions are provided in the following pages.

Table 13-1. PLACE application examples

13.2 DEMO1A.PSF - PA7024

The PLACE design file DEMO1A.PSF incorporates several applications within one design, including: Basic Gates, Basic Registers and Latches, 8-bit Counter, Bi-Directional I/O Port and a Divide-by-2 Clock design. Figures 13-1 and 13-2 show the PLACE pin block and equivalent schematic diagrams.

- **GATES** Basic combinatorial functions including AND, OR, NOR, NAND, EXOR, Inverter, 4-to-1 mux, and 4-bit comparator.
- **REGS** Basic registers including D, T and JK flip-flops with independent clocks, presets and resets, an SR Latch (for debouncing inputs), a gated-latch (LAT1), a basic storage register (REG1), a 2-bit state machine (S0,S1), and a 4-bit shift register (SHF0-3).
- **COUNTER** An 8-bit down counter with Hold, Preset and Reset.
- **PORT** An 8-bit bi-directional I/O port with registered input.

The mode inputs, MODE1 and MODE2, control application selection. Pins A through H are used as inputs and/or control, pins I through P are used as outputs. The outputs of each application are selected via eight 4-to-1 muxes.

Output enable and direction (in PORT mode) are selected by CONTROL.

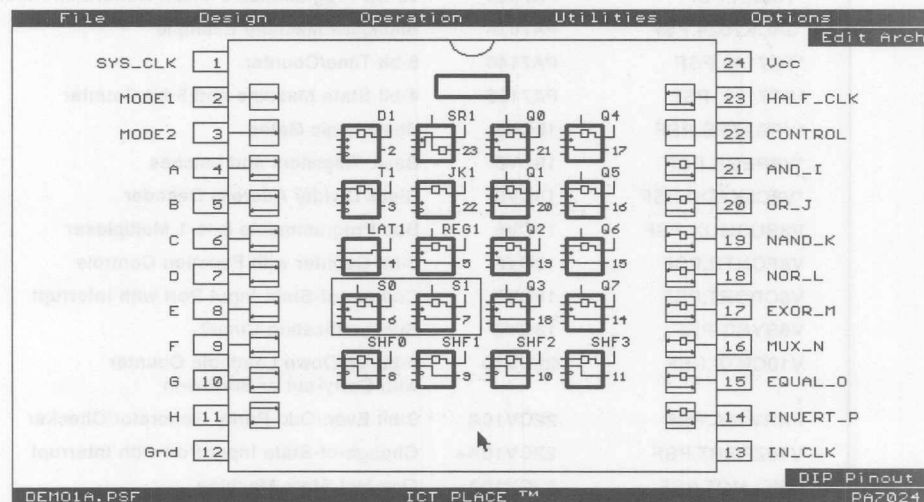


Figure 13-1. PLACE pin block diagram of DEMO1A.PSF

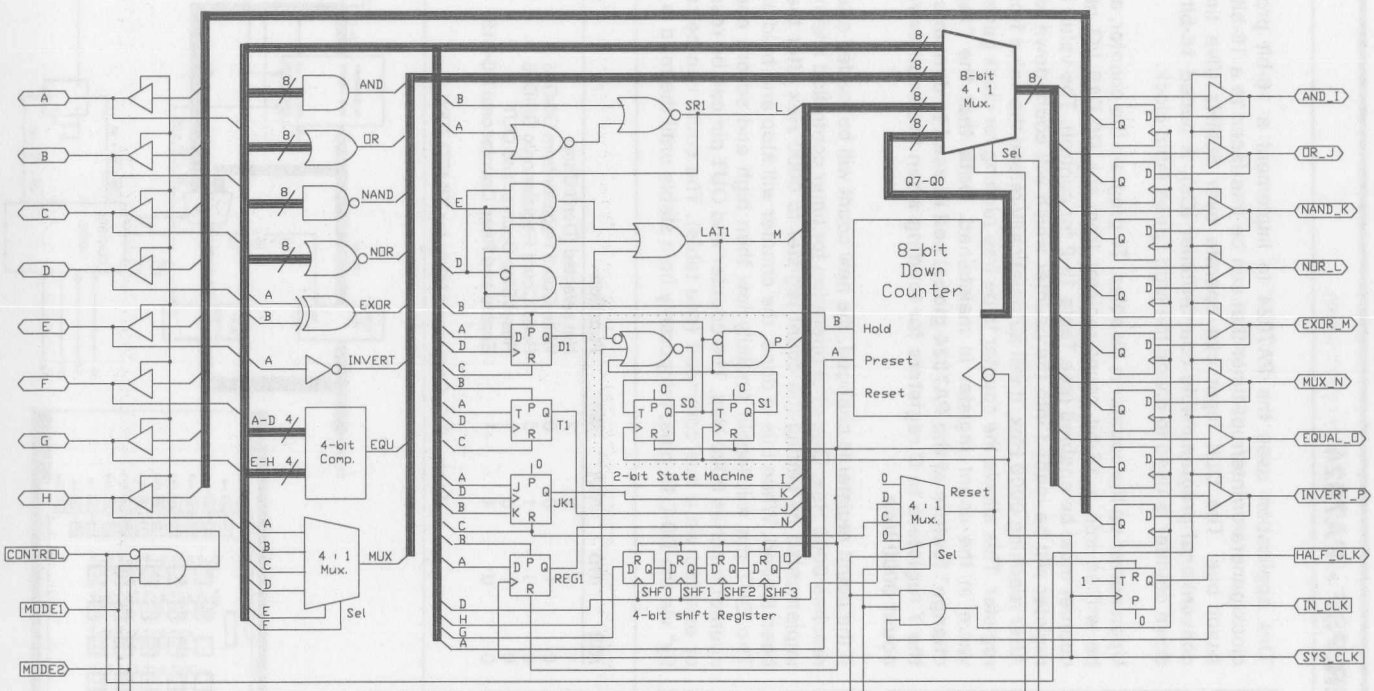


Figure 13-2. Logic schematic of DEMO1A.PSF

13.3 TIMER.PSF - PA7024

This application uses the PA7024 to implement a 16-bit programmable clock-generator/interrupt-timer that can be interfaced to a 16-bit microprocessor bus. The CLK input can operate over 50MHz (five times that of conventional programmable counter/timer ICs). A buried 16-bit reloadable down counter is used to divide the high speed input clock.

Upon power-up the counter is disabled. To program the counter, a value must be written into a 16-bit count register from the D0-D15 I/O pins and the counter must be enabled (see Table 13-2 for control). The value in the count register will be loaded into the counter which will count down to 0000 Hex. After reaching 0000 Hex, it will automatically reload the value from the count register. This allows the counter to be free running for clock generation if the value in the count register is maintained. **Note that the "register-type change" feature of the PA7024 global cell is used to dynamically switch the T registers to D registers for loading when the counter reaches the count 0000 Hex.**

If the count register is changed, the new count will be loaded after the count reaches 0000 Hex. One-shot operation for timer controlled interrupts can be implemented by setting the count register to 0000 Hex after the count has been loaded. When this is done, the counter will stop and hold at 0000 Hex. The OUT pin will toggle (initially low then high and so on) each time the counter reaches 0000 Hex. The counter and OUT pin can be reset, disabled or enabled via a bus command (see table). The count can be read "on the fly" via the D0-D15 pins, temporarily held stable until the read is completed.

/CS	/RD	/WR	/AO	Function
1	X	X	X	Not selected (Don't Care)
0	1	0	0	Write Count Register from D0-D15
0	0	1	0	Read Count Register onto D0-D15
0	1	0	1	Reset/Stop Counter and OUT
0	0	1	1	Enable and Read Counter onto D0-D15

Table 13-2. Command table for TIMER.PSF

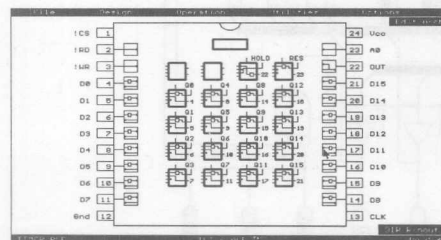


Figure 13-3. PLACE block diagram of TIMER.PSF

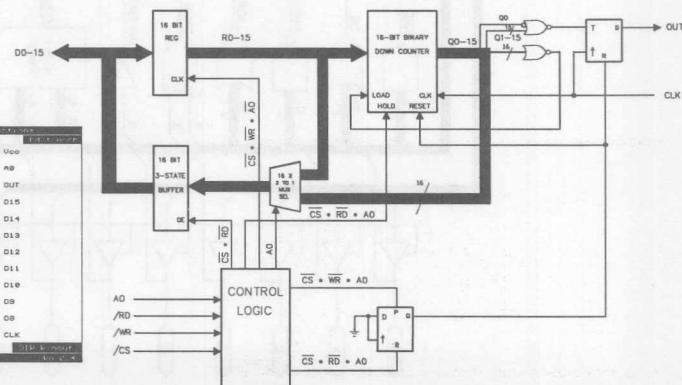


Figure 13-4. Logic schematic of TIMER.PSF

13.4 JACK7024.PSF - PA7024

This design example is based on C.R. Clare's design in Designing Logic Systems Using State Machines (McGraw Hill, 1972). The blackjack machine plays the dealer's hand, using typical dealer strategies to decide whether to draw another card (hit) or stand after each round.

The example contains the following logic designs:

- A state machine that controls the game logic which includes:
 - checking the status of the card reader.
 - making the decision of what action to take for a hit, stand or a bust. An example is to draw a card if the hit signal is true.
 - making the decision of when to use the value 1 or 11 for an ace card.
- A Multiplexer/Comparator which compares the point total and sends the hit, stand or bust signal to the state machine. If the point total is greater than 21, it's a bust. If it is equal or less than 16, then hit, else stand.
- A 5-Bit Adder that adds the value of the drawn card.
- A Binary-to-BCD converter for converting the 5-bit binary score and converts it to 2-digit BCD for the digital display.

This design example can also be implemented by using three PLDs which include a PAL22V10 for the Multiplexer, Comparator and Adder, a PAL16L8 for the Binary-to-BCD converter, and a PAL16R6 for the state machine.

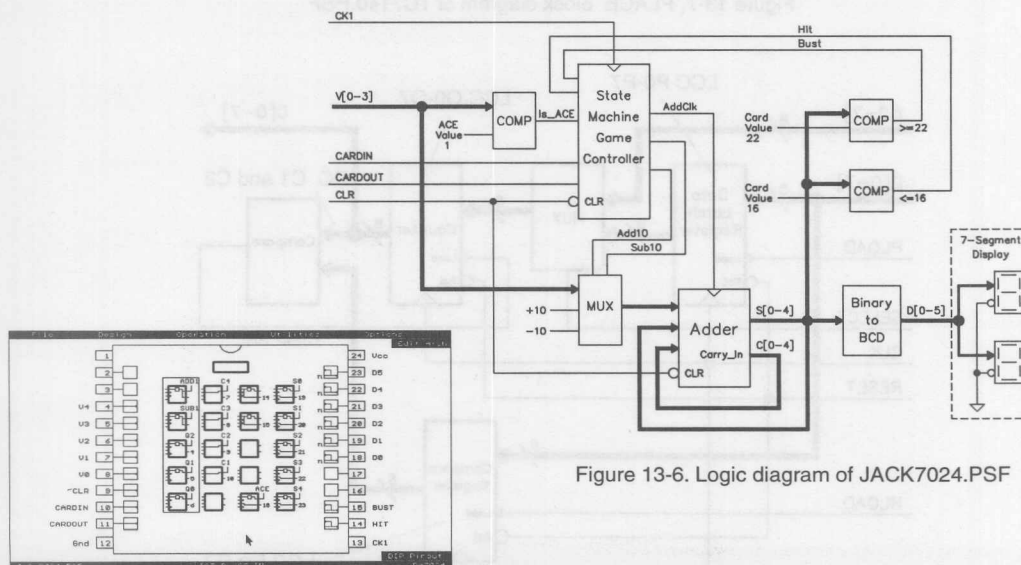


Figure 13-5. PLACE block diagram of JACK7024.PSF

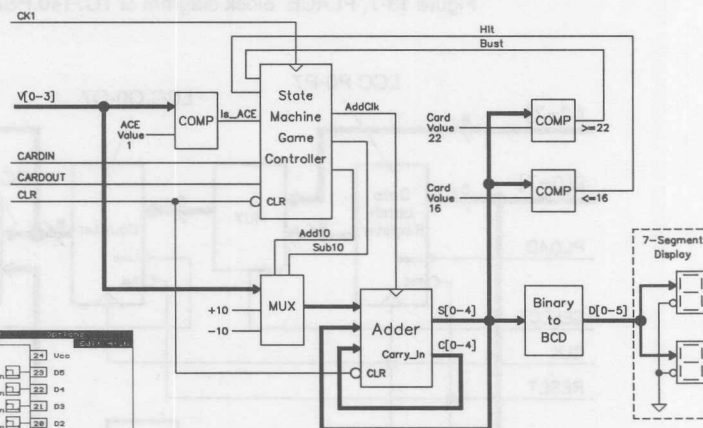


Figure 13-6. Logic diagram of JACK7024.PSF

13.5 TC7140.PSF - PA7140

This example uses a PA7140 device to implement a timer/counter application which is typically used in a microprocessor-based computer system. The circuit employs a multiplexer to allow either the incoming or latched data to be loaded into the counter. The desired data is then loaded into the counter either by resetting the counter and the compare register, or by a match between the counter's state and the value in the compare register.

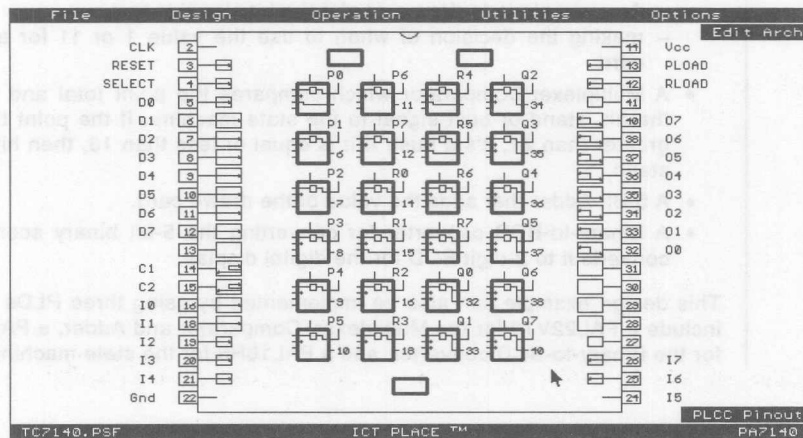


Figure 13-7. PLACE block diagram of TC7140.PSF

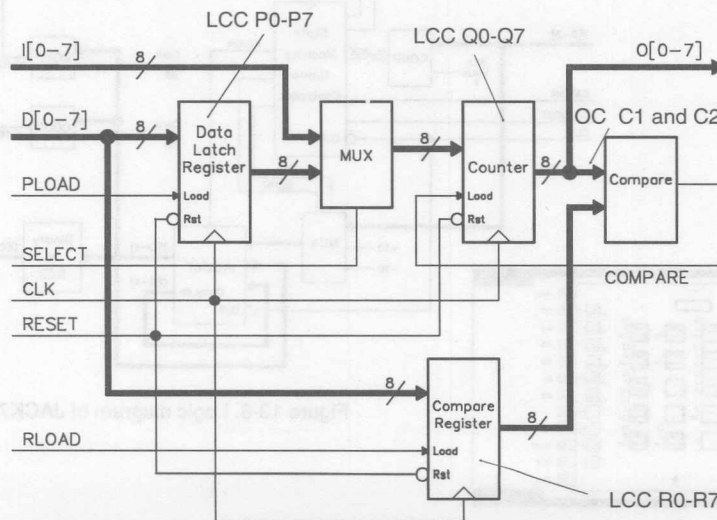


Figure 13-8. Logic diagram of TC7140.PSF

13.6 ST7128.PSF - PA7128

This example implements an 8-bit buried counter, an 8-bit buried register, and a 4-bit buried state machine. The counter uses 8 LCC registers and the 8-bit register and 4-bit state machine uses 12 IOC register/latches. IOC registers can be buried by using the feature of the PA7128 that allows the output enables to be fed back into the array.

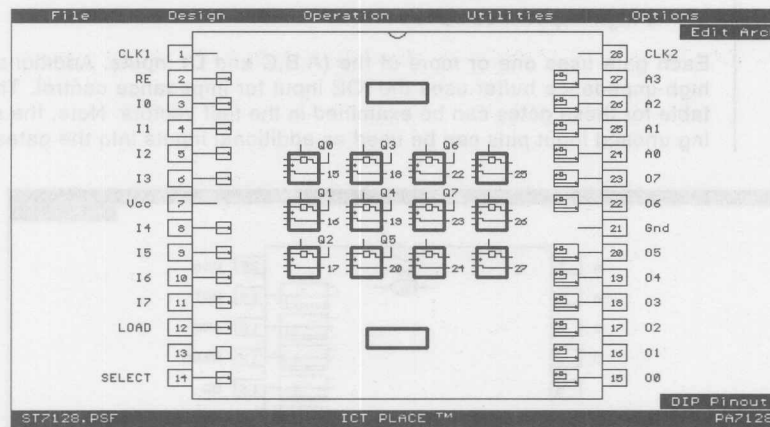


Figure 13-9. PLACE pin block diagram of ST7128.PSF

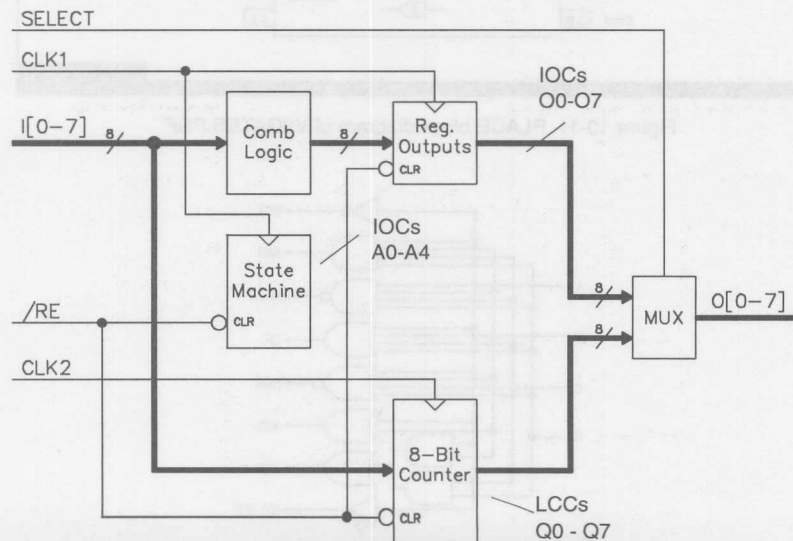


Figure 13-10. PLACE logic diagram of ST7128.PSF

13.7 V8GATES.PSF - PEEL18CV8

This PEEL18CV8 application example implements several basic logic gates. The logic gates include:

- an inverter
- four-input AND, OR, NAND, and NOR gates
- a four-input AND-OR-INVERT gate
- a two-input XOR gate
- a high-impedance buffer.

Each gate uses one or more of the (A,B,C and D) inputs. Additionally, the high-impedance buffer uses the /OE input for impedance control. The truth table for these gates can be examined in the test vectors. Note, the remaining unused input pins can be used as additional inputs into the gates.

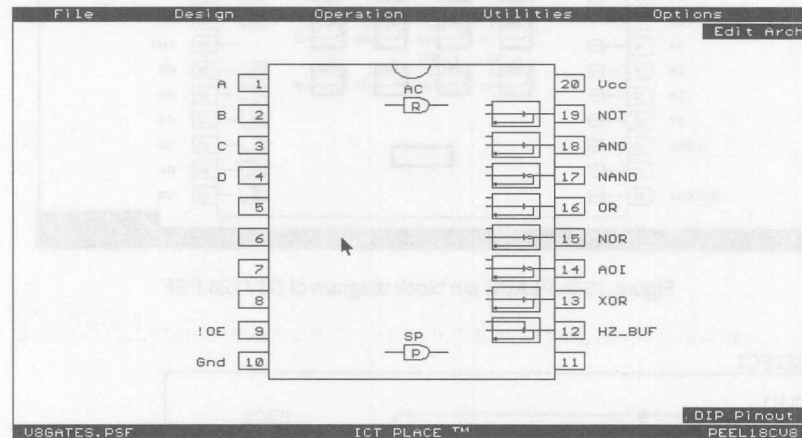


Figure 13-11. PLACE block diagram of V8GATES.PSF

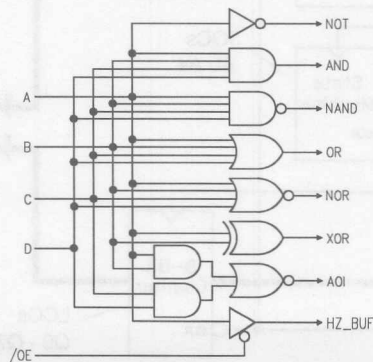


Figure 13-12. Logic schematic of V8GATES.PSF

13.8 V8REGS - PEEL18CV8

This application example demonstrates the implementation of several basic registers and latches within a PEEL18CV8. Four register types included are the D, T, JK, and SR, all of which are clocked by the CLK input. All registers can be synchronously reset, set, and asynchronously reset using the SRES, SSET and ARES inputs respectively. Besides the registers, an SR latch and a Gated Latch circuit show how independent asynchronous storage elements can be implemented. Only the Q outputs of these registers and latches are provided at the output pins. The /Q outputs could easily be accessed by inverting the macrocell output polarity. Truth table operation can be referenced via the test vectors.

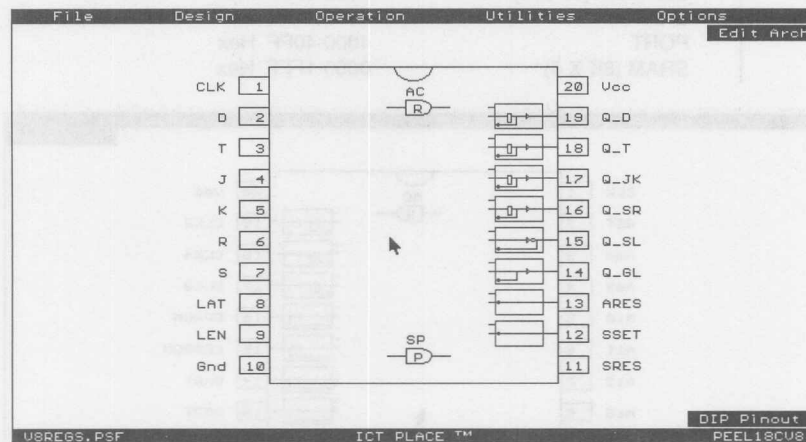


Figure 13-13. PLACE block diagram of V8REGS.PSF

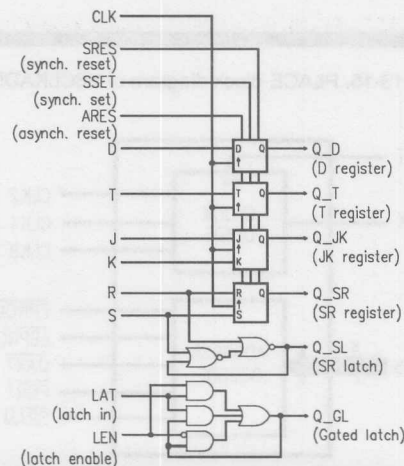


Figure 13-14. Logic schematic of V8REGS.PSF

13.9 V8CLKADD.PSF - PEEL18CV8

This application uses the PEEL18CV8 for two common microprocessor system functions: a clock divider and a memory mapped address decoder. The clock divider provides $\div 2$, $\div 4$ and $\div 8$ clock outputs. The SET input sets all clock outputs high. The address decoder decodes the processor address lines to select one of five memory or I/O devices. The chip select for these devices are active low. The memory map over a 64K boundary is shown below.

Memory Map for Address Decoder

Function	Address
EPROM (32K X 8)	8000-FFFF Hex
EEPROM (2K X 8)	5000-5FFF Hex
UART	4100-41FF Hex
PORT	4000-40FF Hex
SRAM (8K X 8)	0000-1FFF Hex

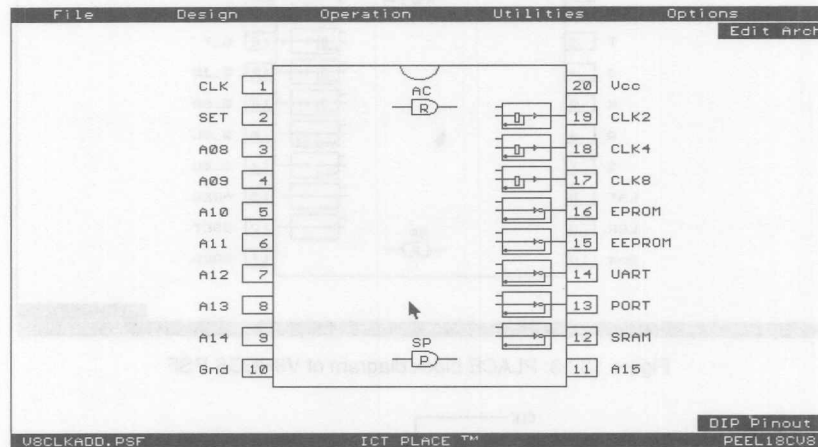


Figure 13-15. PLACE block diagram of V8CLKADD.PSF

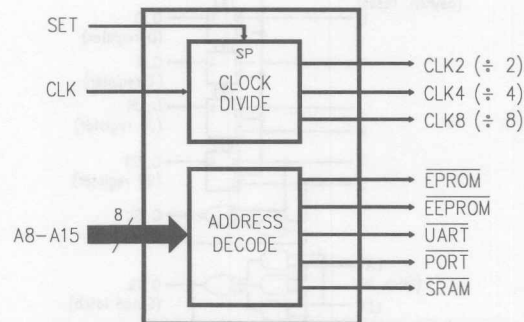


Figure 13-16. Block diagram of V8CLKADD.PSF

Sales Representatives and Distributors

ICT North American Sales Offices A-3
North American Sales Representatives A-3
North American Distributor Network A-4
ICT International Sales Representatives A-6

Sales Representatives and Distributors

ICT North American Sales Offices	A-3
North American Sales Representatives	A-5
North American Distributor Network	A-4
ICT International Sales Representatives	A-6